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Chip-to-Wafer Technologies for High Density 3D Integration

2007

CEA Leti Minatec Campus,
STMicroelectronics,
SET, CNRS Cemes,
Air Liquide Electonics Systems

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A collaborative work

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Chip-to-Wafer Technologies for High Density 3D Integration

Introduction

Direct Cu bonding process

SET FC300 with special design

Alignment performance

Electrical validation

Conclusions

3D assembly by chip or wafer stacking

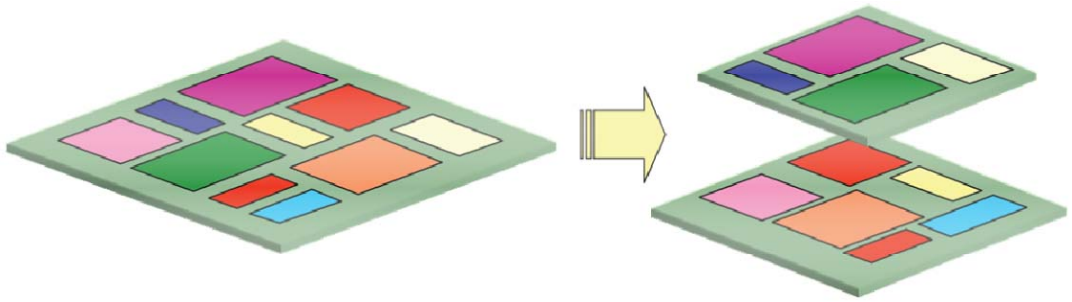
Multifunction devices (heterogeneous integration)

Repartitioning

reduces area of individual chips (Yield improvement).

reduces number of mask levels per die (Cost improvement).

results in shorter global interconnect lines (Energy saving / performance improvement).



Chip-to-Wafer stacking through direct bonding

Flexibility

- In size
- In technology / supplier

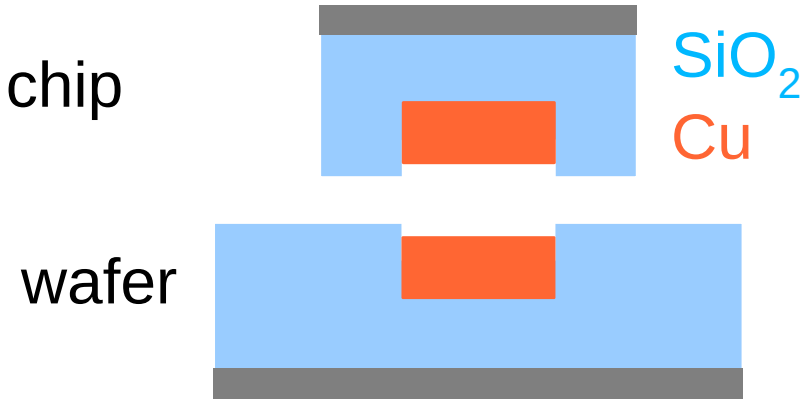
High yield

- Known good dies
- Good overlay

Benefits of direct bonding

- Low pressure
- Low temperature
- No underfill even at high interconnect density

Die-to-Wafer alignment

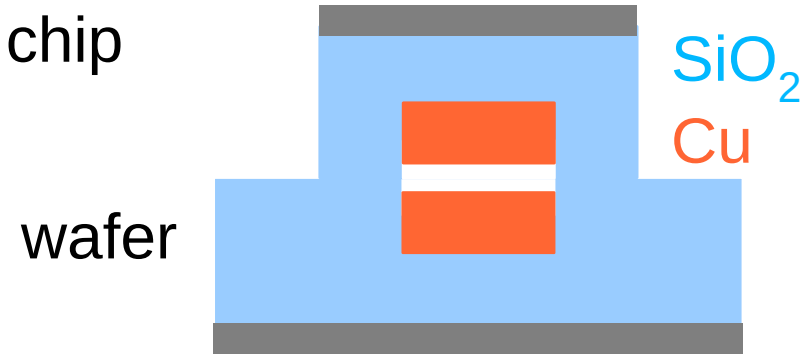


Damascene processing determines die and wafer surface topography.

Cu surface is recessed (dishing).

Both chip and wafer surfaces are activated prior to bonding.

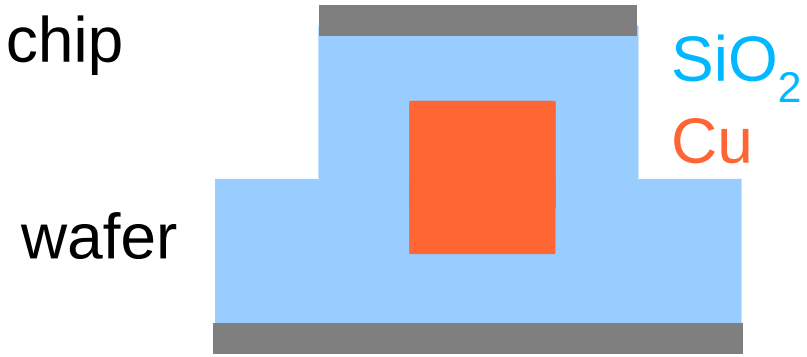
Die-to-Wafer placement



Die is placed.

Die is secured by direct SiO_2- SiO_2 bonding (low force, room temperature).

Die-to-Wafer interconnection



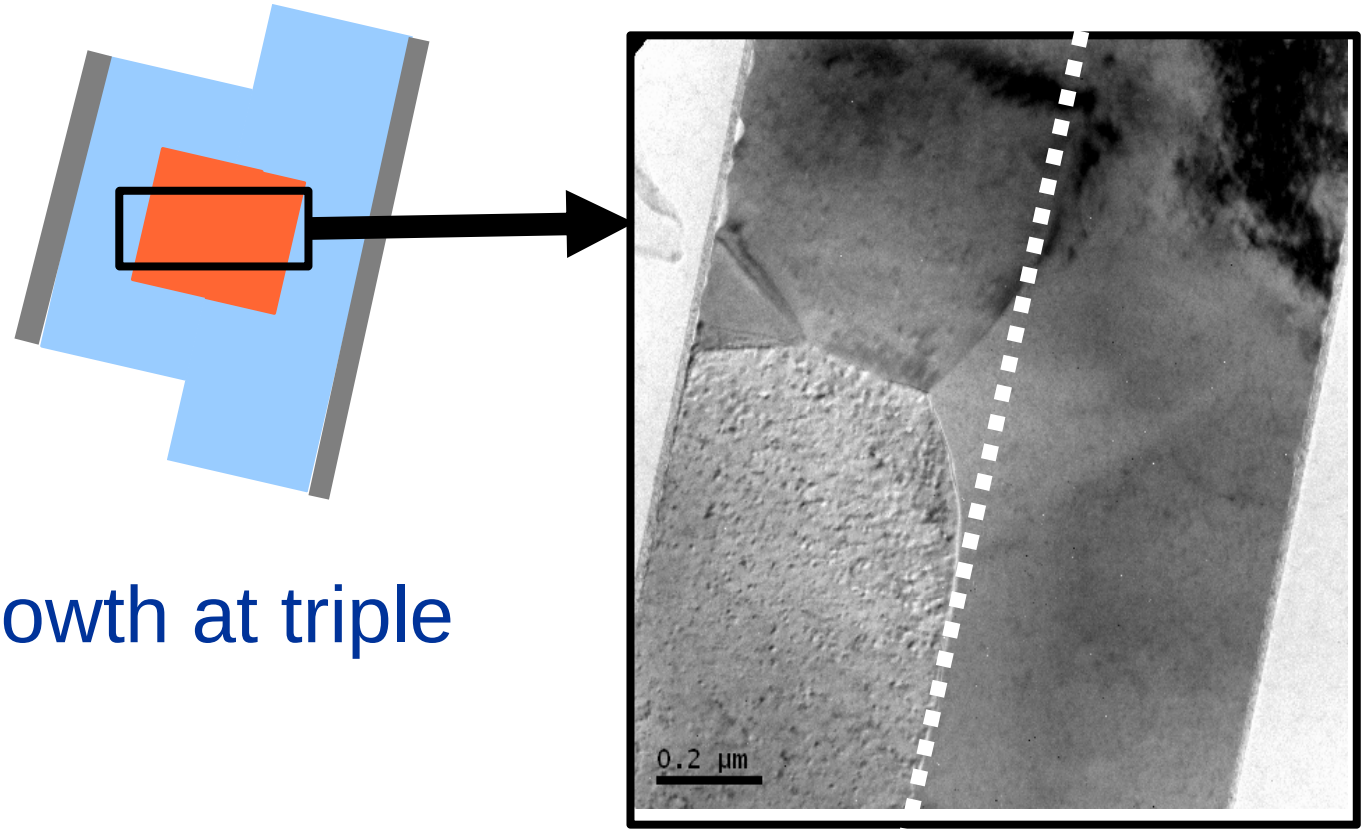
Cu - Cu direct bonding:

occurs during collective annealing.

is driven by Cu thermal expansion.

depends on Cu thickness, dishing and temperature.

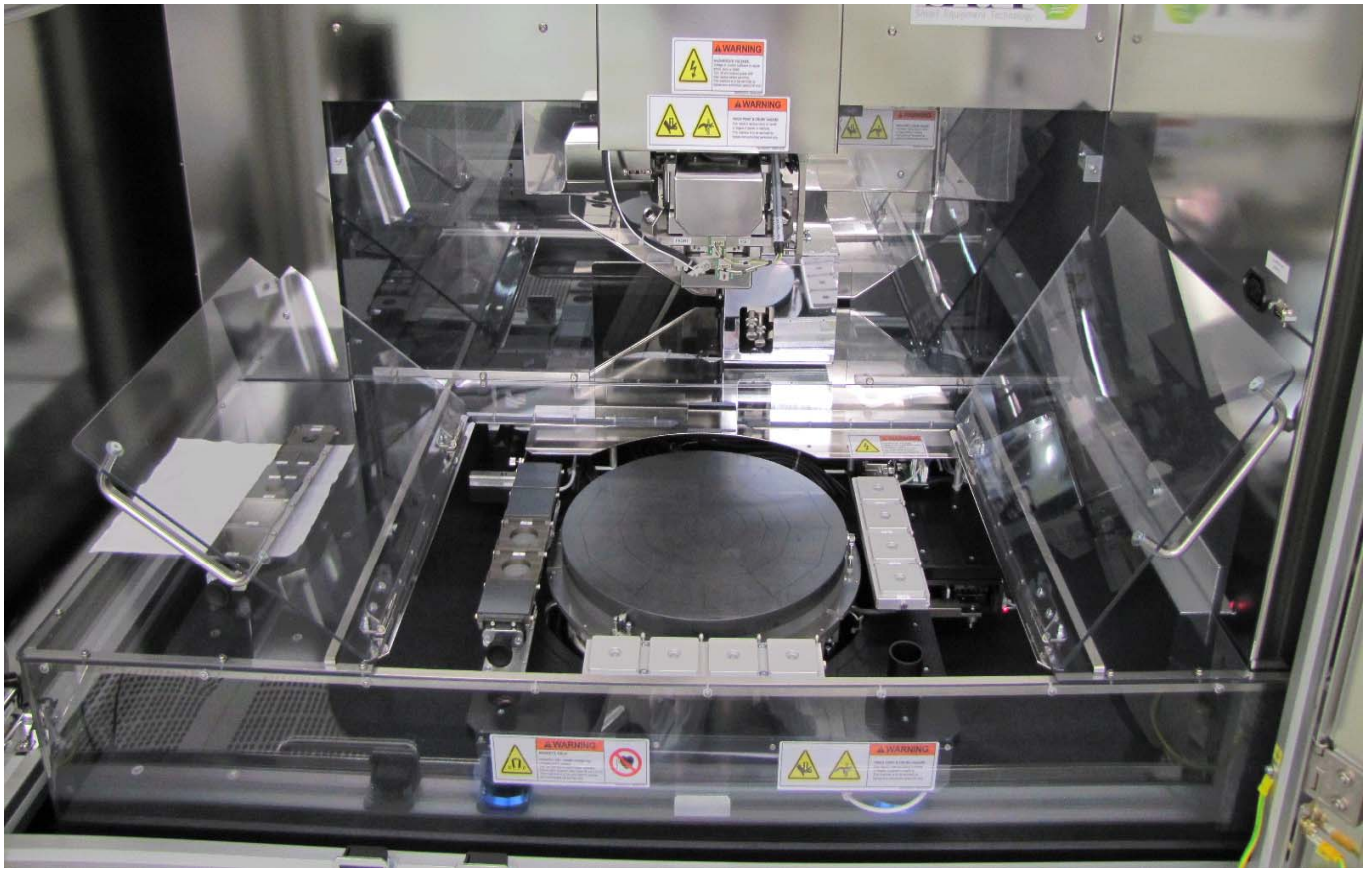
Grain boundaries evolve with annealing.



Grain growth at triple points

Here: 2h @ 400ºC

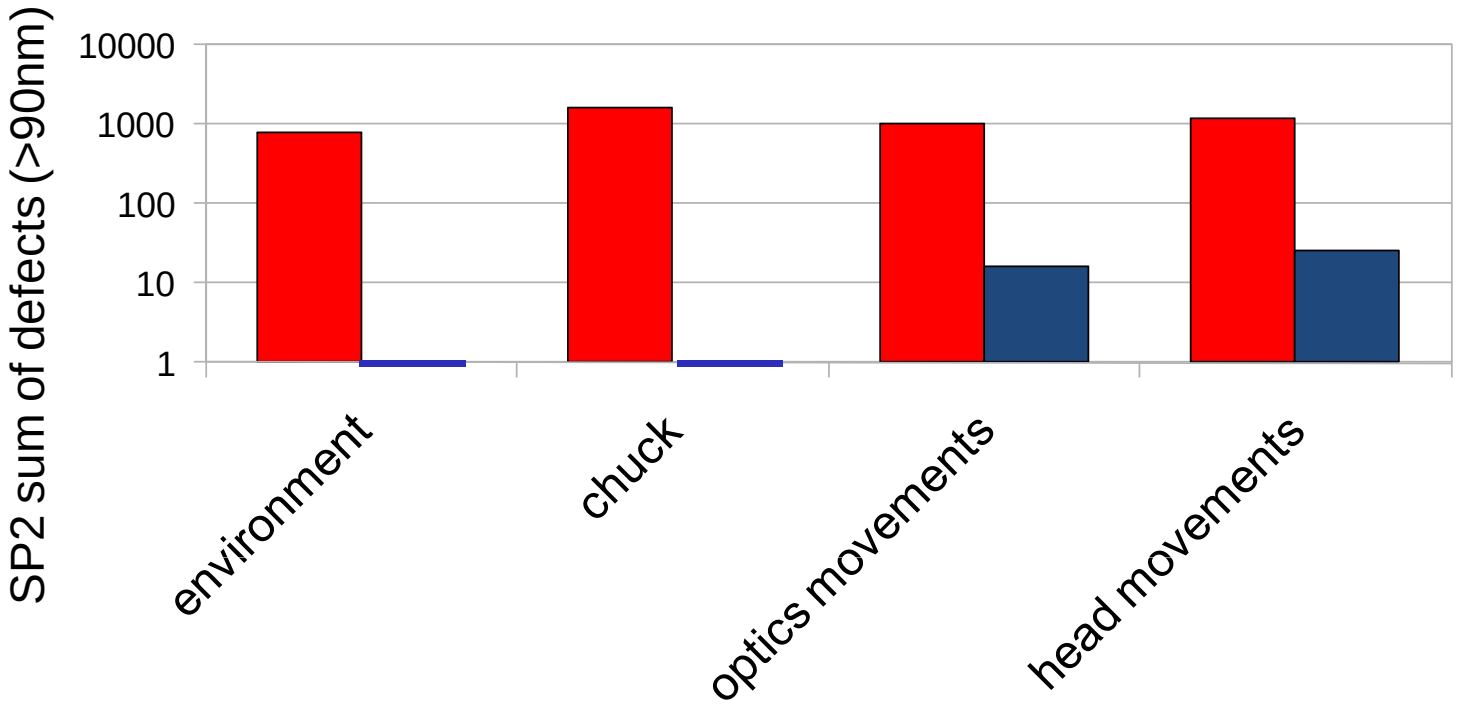
FC300 special design against particulate contamination



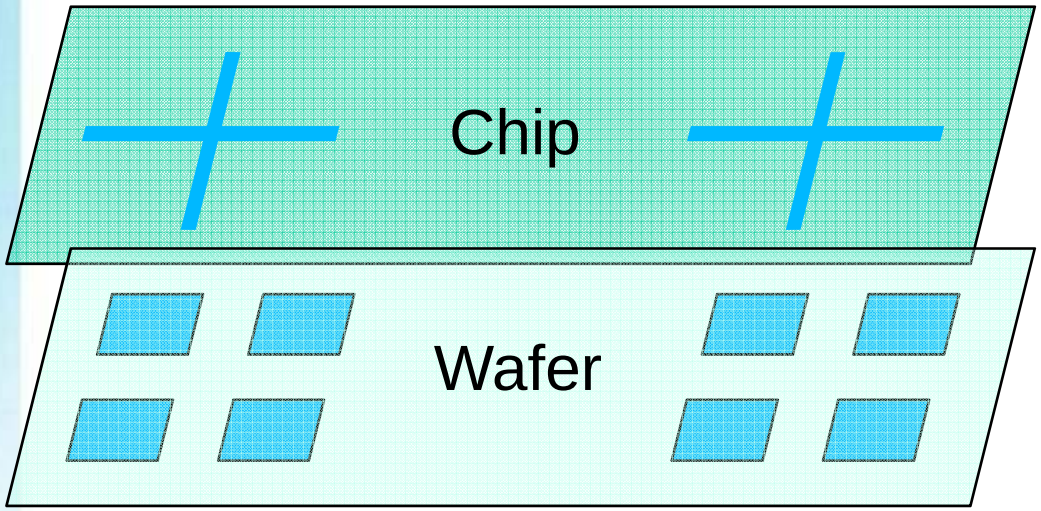
Effective particulate contamination control with special design FC300

FC300
in class 1000 environment

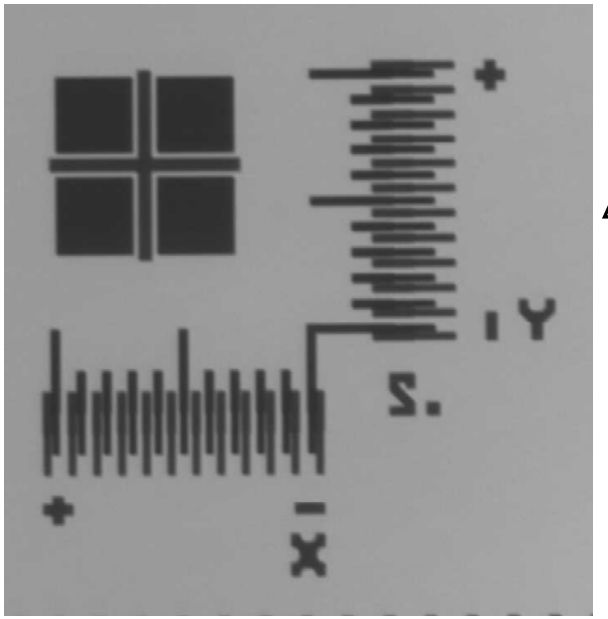
special design FC300
in class 10 environment



Alignment control



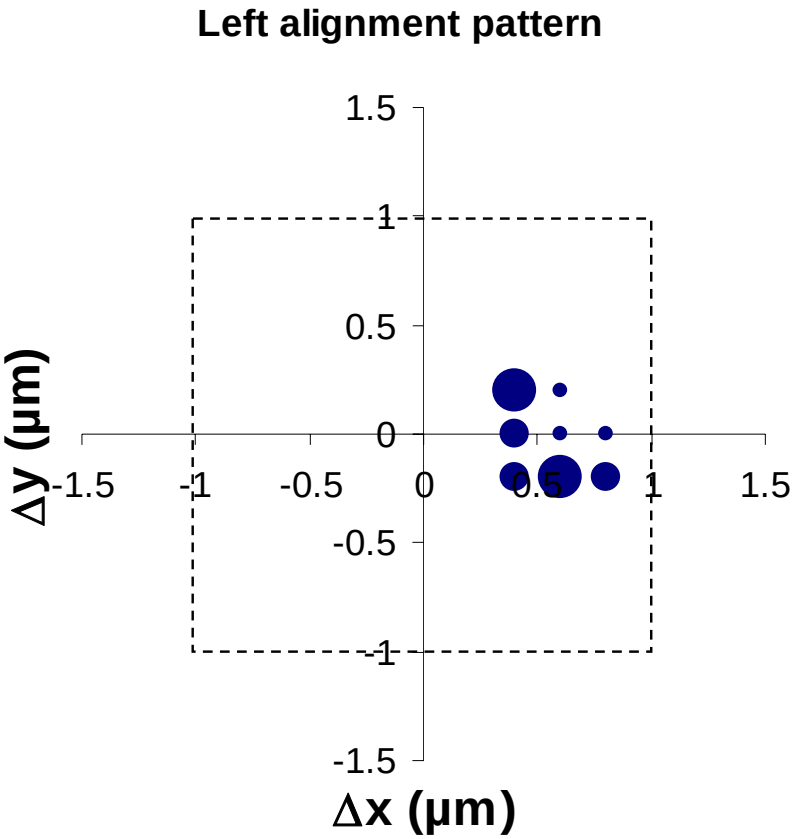
Infrared reading

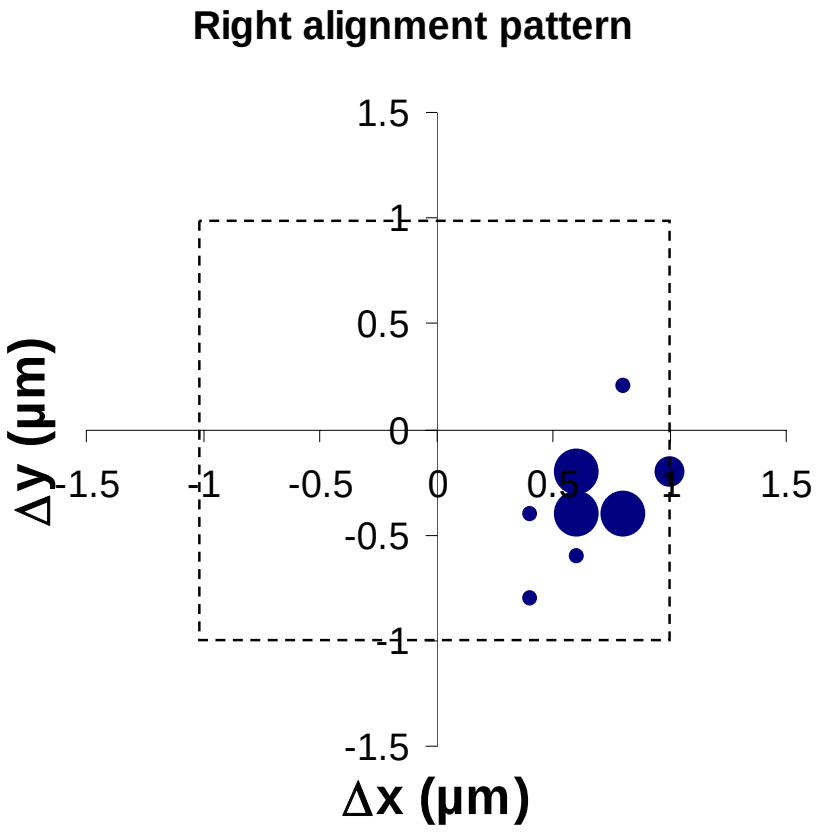


Δy

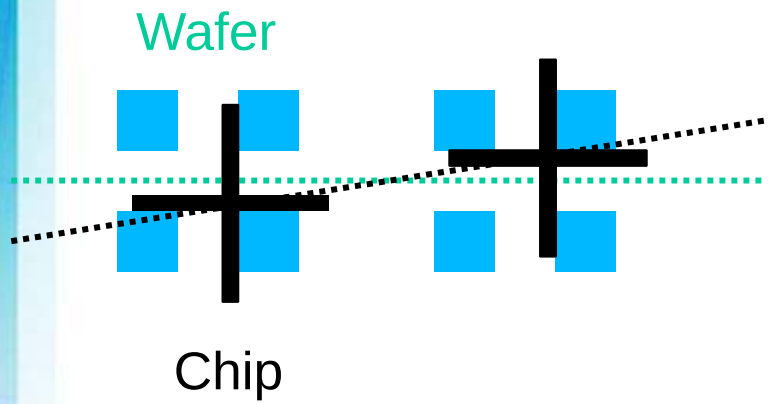
Δx

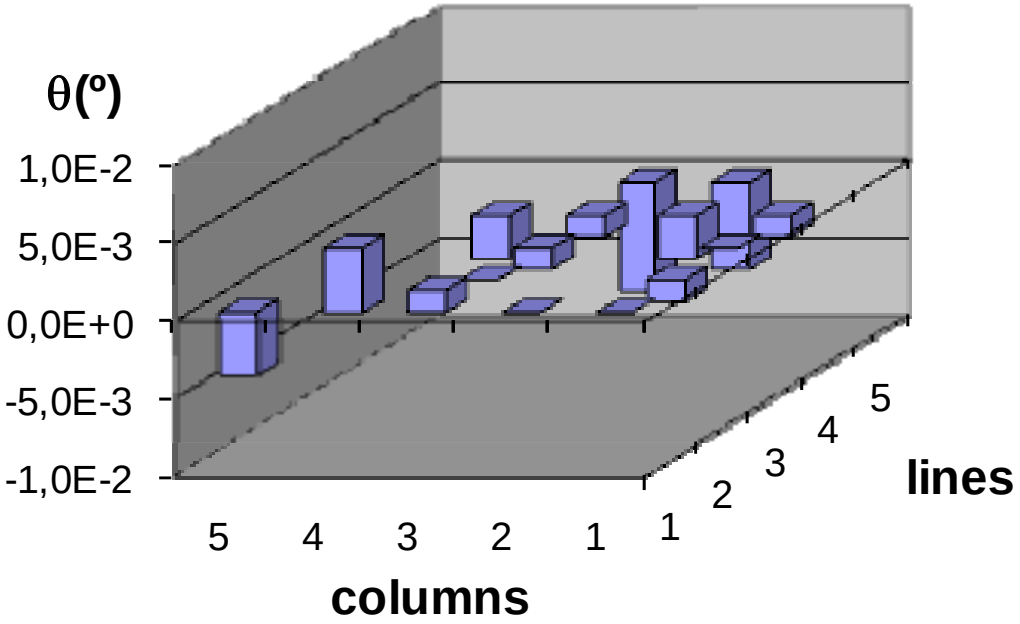
Axial alignment is controlled ≤ 1 µm and could be improved by working on calibration.



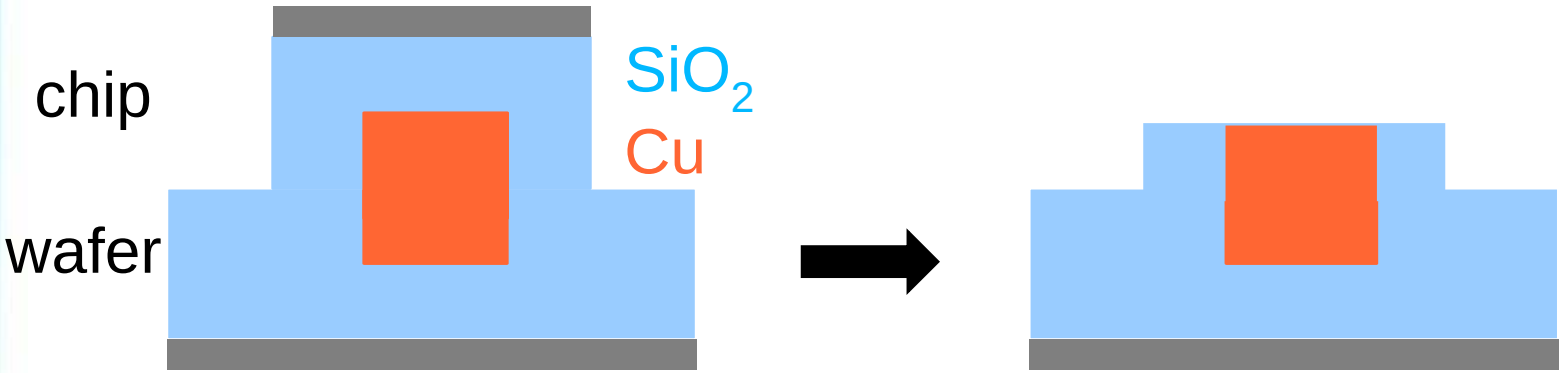


Angular misalignment < 10^{-2} degree





Sample preparation for electrical measurements



Si coarse grinding

Si etch (TMAH)

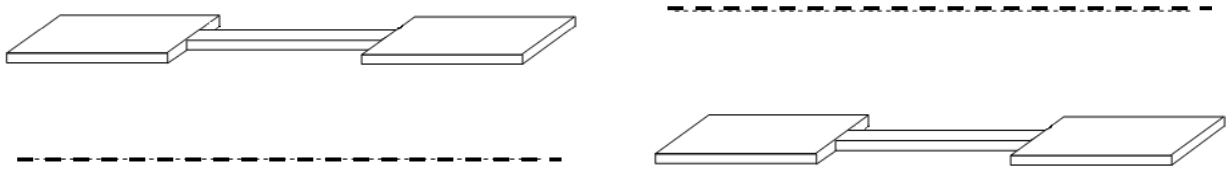
SiO_2etch

Cu resistivity is as expected on each level.

L=640µm
W=3µm
T=0.5µm

chip

wafer



ρ = 21.7 ±0.2 nΩ·m

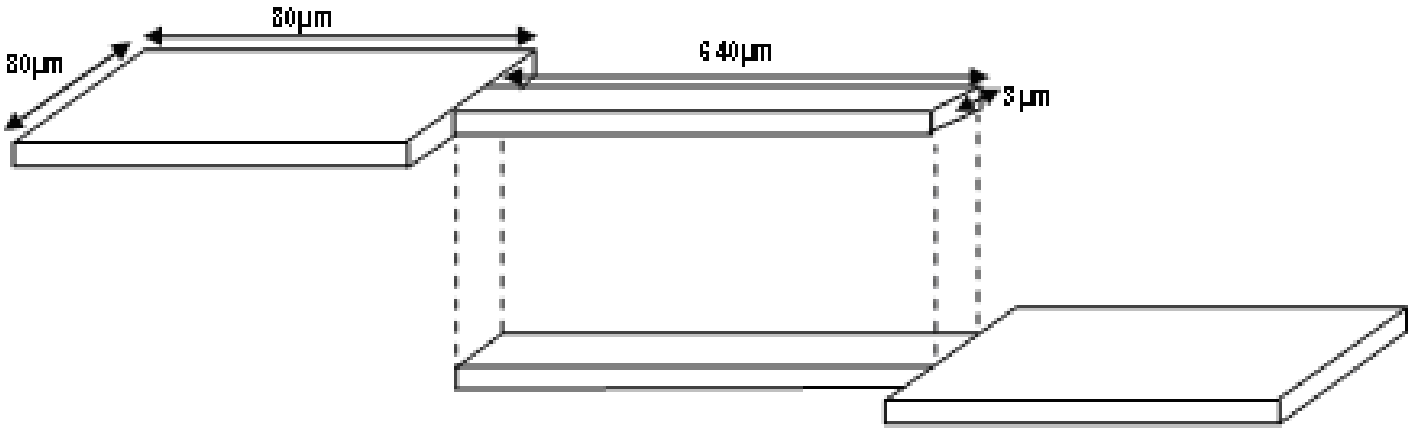
ρ = 20.8 ± 0.2 nΩ·m

Current flow from Chip to Wafer

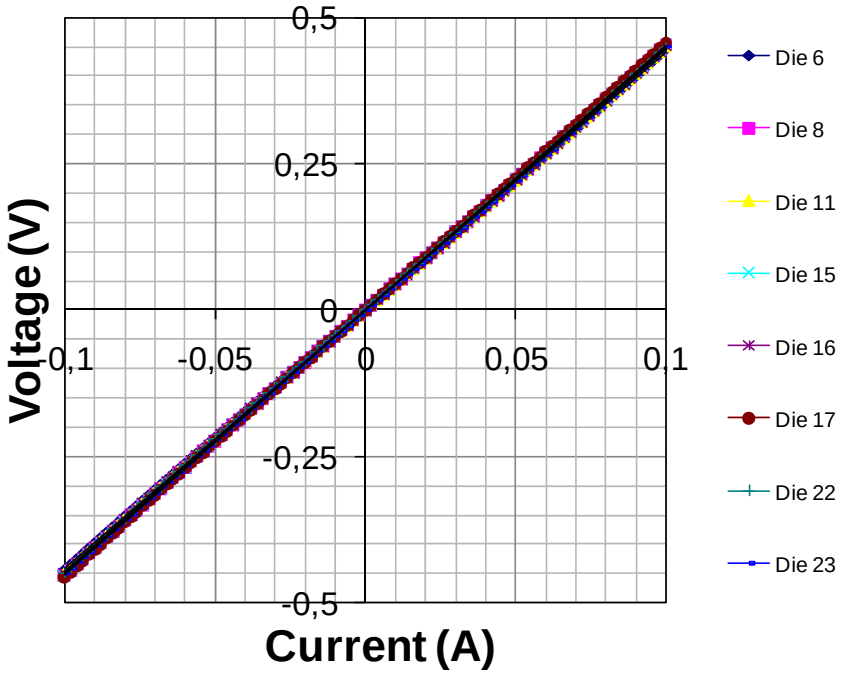
L=640µm
W=3µm
T=2x0.5µm

chip

wafer



Bonded interconnects show identical resistivity as for Wafer-to-Wafer bonding

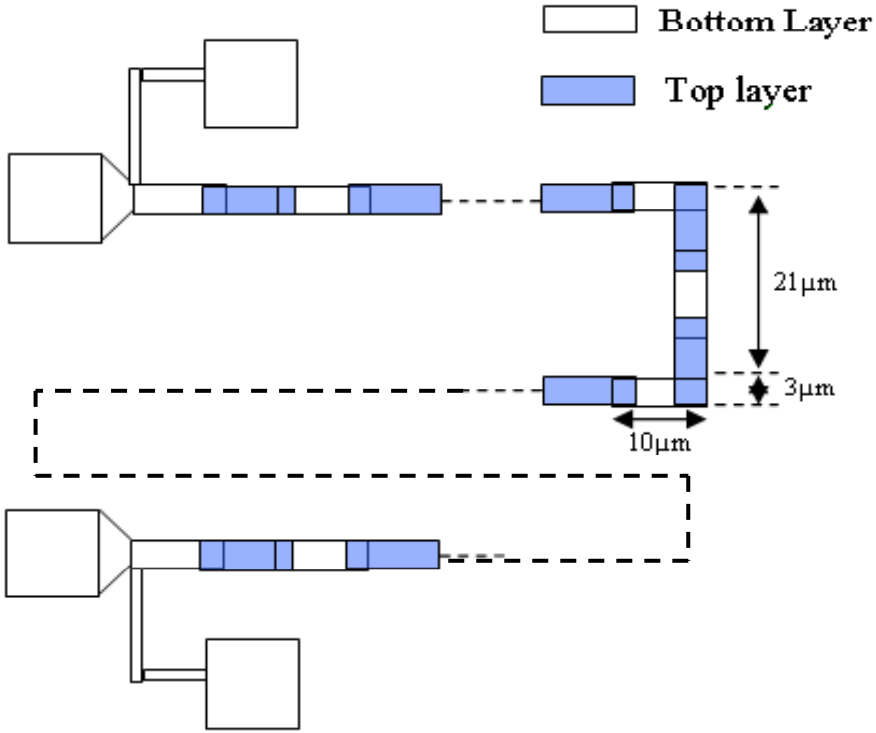


$\rho = 20.9 \pm 0.2\ n\Omega{\cdot}m$

$\rho = 20.8\ n\Omega{\cdot}m$ on Cu-Cu bonded wafers:

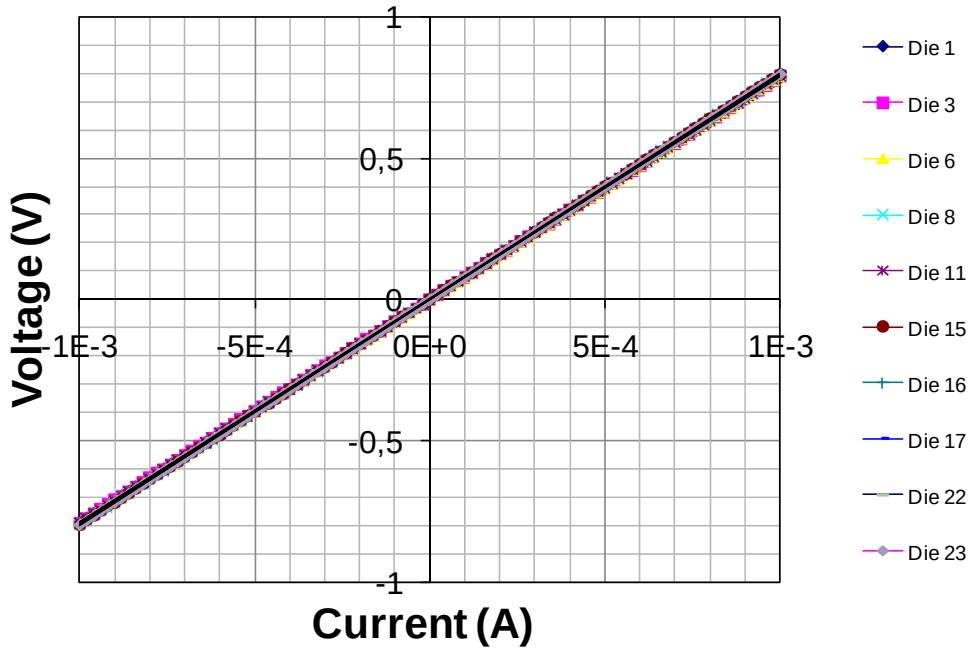
R. Taibi *et al.*, "Full characterization of Cu/Cu direct bonding for 3D integration", *Proceedings 60th ECTC*, pp.219-225, June 1-4 2010

Current flow through multiple bonding contacts



There are **10136** bonding contacts (3x3 µm²) with 7 µm pitch.

The long daisy chain shows very tight resistance distribution.



$\rho = 24.3 \pm 0.2\ n\Omega \cdot m$

This resistivity value probably contains a contribution from the bonding interface.

Conclusions

Chip-to-Wafer assembly has been demonstrated through Pick & Place and direct Cu-Cu bonding.

The benefit of the approach is to allow low temperature and low pressure die positioning, and to work without underfill even at high interconnect densisties.

FC300 special design effectively reduces particulate contamination. Misalignment is ≤ 1 µm and could be reduced by improving the calibration procedure.

Chip-to-Wafer electrical continuity was verified for the first time and is showed to behave as in Wafer-to-Wafer configuration. Characterization is on going and further results will be submitted to IEDM 2011 (R. Taibi *et al.*).

Acknowledgments

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