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UV nanoimprint lithography process optimization for electron device manufacturing on nanosized scale

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Motivation

Fabrication of electron devices (short channel MOSFETs) by UV nanoimprint lithography (UV NIL) and conventional silicon (Si) semiconductor processes like reactive ion etching (RIE) and optical lithography.

Already accomplished UV NIL optimizations from earlier works

- Fabrication of UV NIL templates [1]
- Adhesion of the nanoimprint resist (UV polymer) to the template and the substrate [2]
- Life time of the antisticking layer [1]

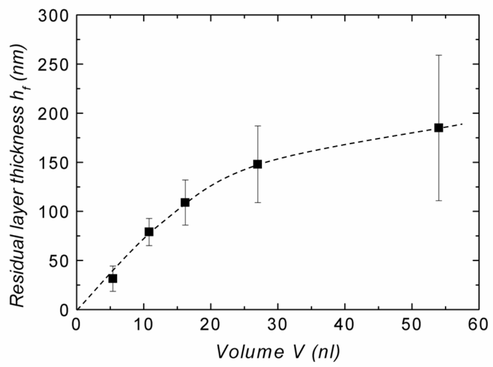
Current tasks for UV NIL optimization and electron device manufacturing

- Thin and uniform residual layer thickness (RLT)
- Removal of the RLT and pattern transfer into the substrate by RIE
- Compatibility to conventional Si semiconductor processing and Si process optimization

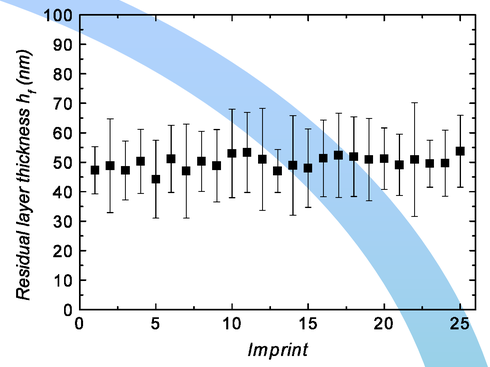
Thin and uniform residual layer thickness

Integration of a multidrop ink-jet system into the imprint stepper NPS300 from S.E.T. (formerly SUSS MicroTec).

- Drop pattern and volume optimization
- Evaluation of the uniformity of the RLT



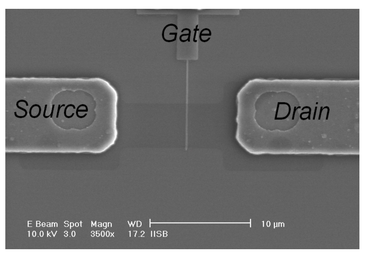
Residual layer thickness for different amounts of dispensed UV polymer.



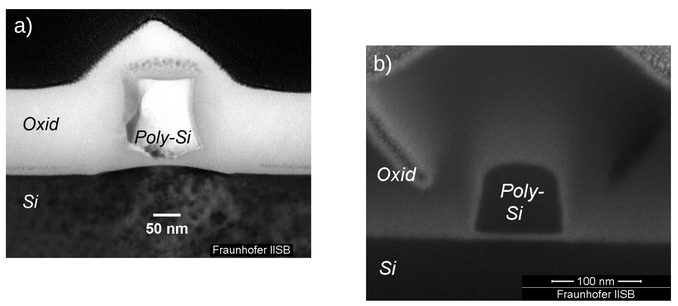
Residual layer thickness for 25 imprints on a poly-Si layer, deposited on an oxidized 150 mm Si substrate. The patterned UV polymer on the substrate was used to subsequently etch poly-Si gates of short channel n-MOSFETs. The UV polymer used was NIF-A-5b from Asahi Glass Company.

Optimization of the UV polymers viscosity and etch resistance together with Asahi Glass Company.

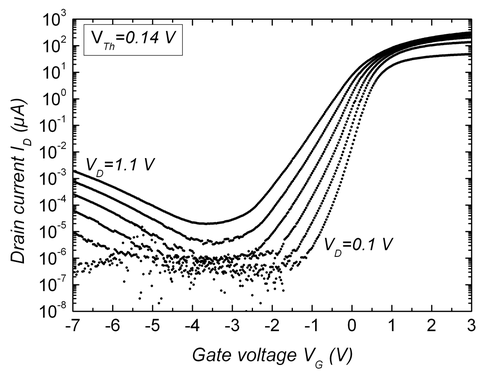
Compatibility to conventional Si semiconductor processing and Si process optimization



SEM image of a manufactured short channel n-MOSFET.



Cross section images of poly-Si gates, patterned by UV NIL and RIE a) before (TEM image) and b) after Si process optimization (SEM image). The poly-Si gates are part of short channel n-MOSFETs with a channel length of around 90 nm.

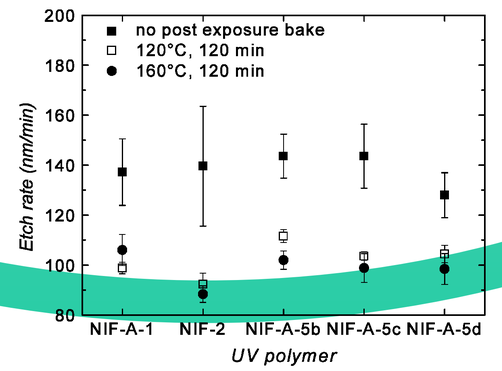


Transfer characteristic of the optimized short channel n-MOSFET with a channel length of 90 nm.

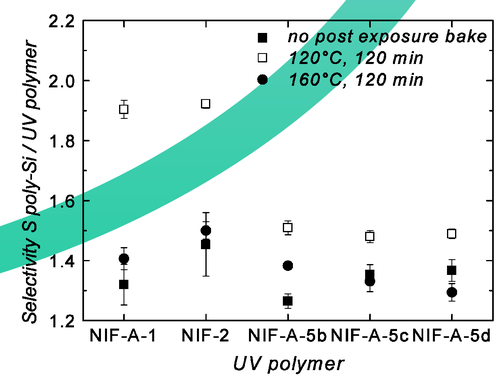
Combination of UV NIL patterning with conventional Si semiconductor processes. Optimization of Si semiconductor processes to finally manufacture short channel MOSFETs.

Removal of the RLT and pattern transfer into the substrate by RIE

- RIE process and UV polymer post exposure baking optimization



UV polymer etch rates for different post exposure bake conditions against the RLT etching process.



UV polymer etch resistances for different post exposure bake conditions against the poly-Si etching process.

Conclusion

- UV NIL is compatible to conventional Si semiconductor processing and is applicable for future electron device manufacturing

[1] H. Schmitt, M. Zeidler, M. Rommel, A.J. Bauer, H. Ryssel, Microelectron. Eng. 85 (2008) 897-901
[2] H. Schmitt, L. Frey, H. Ryssel, M. Rommel, C. Lehrer, J. Vac. Sci. Technol. B. 25 (2007) 785-790

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