New Reflow Soldering and Tip in Buried Box (TB2) Techniques For Ultrafine Pitch Megapixels Imaging Array

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Abstract

Flip chip is a high-density and highly reliable interconnection technology which is mandatory for the fabrication of high end heterogeneous imaging arrays. The control of ultra-fine pitch (<10 µm) and high bumps count flip-chip bonding technology represents a challenge on the roadmap of next generation devices [1].

This paper describes and compares in details two new flip-chip technologies that can address the challenges at the 10 µm pitch node: a modified reflow soldering technology and a thermocompression "tip in buried box" (TB2) insertion technology.

The technological preparation of the flip-chipped devices is fully described including new maskless underbump metallization (UBM) technique, new maskless soft solder buried box filling technique and new "micro-tube" fabrication technique.

First the flip chip experiments are described as well as two methods to evaluate minimum insertion force for the TB2 technology: 500x500 area arrays insertion/ pull out forces are measured as well as original "single tip into solder" insertion/ pull out forces.

The reduction of the required thermocompression forces obtained with "micro-tube" is demonstrated, finally first reflow and thermocompression hybridization results are achieved and commented.

1. Introduction

Today, two types of flip chip techniques are generally performed for the assembly of high complexity imaging arrays: the "reflow soldering" [2] and the "thermo-compression" technique. However, both techniques present specific issues regarding hybridization yield, most of which are related to planarity and warping of devices to be assembled. In standard reflow soldering approach, planarity defects can be compensated by the relative geometry of the bumps and the wetting surfaces [3]. However, below 10µm pitch the increasing number of interconnection (i.e. device size) and the smallest size of the bumps are not favorable to balance planarity defects, inducing defects such as unconnected bumps. On the other hand, standard thermo-compression technique reduces planarity issues by using force and plastic deformation of solder bumps to compensate non-planarity. However, any parallelism or local non-planarity defects can induce local over-pressure and generate shorted bumps during thermo-compression.

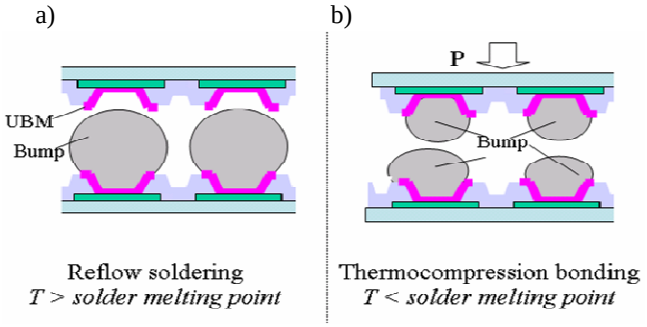


Fig. 1 Flip-chip techniques: a) reflow soldering, b) thermocompression

2. New approaches

In this paper, we investigate and compare two new flip-chip approaches using micro-tips to achieve ultrafine pitch (< 10 µm) and high bumps count (2000x2000 interconnections): a new reflow soldering flip-chip process and a "Tip in Buried Box" (TB2) insertion technology [4].

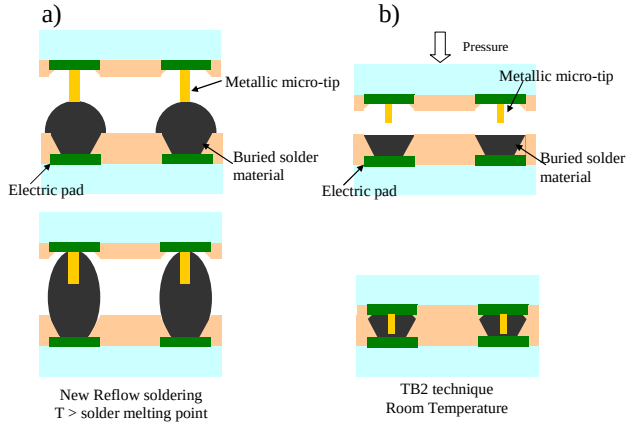


Fig. 2 A new reflow soldering technique (a) and TB2 proprietary technique (b)

A Description of the modified reflow soldering approach (Fig. 2a)

Flip-chip elementary joining is no more achieved between bumps and a planar under bump metallization (UBM) (Fig. 1a) but between bumps and micro-tips used as wicks during the reflow soldering step (Fig. 2a). This improved technology aims at balancing the planarity defects and bumps non-uniformity by the use of a metal micro-tip as a wick for the solder wetting. This technique described in [5] raises the

acceptance level of chip's surfaces non-co-planarity by increasing temperature slightly over solder melting point.

B Description of the TB2 technology approach (Fig. 2b)

Reflow soldering technique requires the use of chemical flux to break solder oxide during soldering; this may require a costly post-soldering cleaning step. To solve this problem, TB2 technology proposes to break the native solder oxide film by using fluxless physical insertion. Electrical connections are performed by the insertion of conductive micro-tips in ductile material (Fig. 2b). After the initial alignment step, metal micro-tip is inserted into solder box. Thanks to the micro-tips geometry and the indium ductility, the applied pressure can be compatible with conventional Flip Chip bonding equipment. Also, the bonding step can be performed at room temperature followed by solid-solid diffusion [6].

Next sections describe the different processes developed to prepare chips for these two new types of hybridization as well as the development of the hybridization techniques themselves.

3 Experimental study

3.1 Under Bump Metallization (UBM) fabrication

The UBM material stack is directly fabricated and self-aligned to passivation openings (vias) delivered chips. For example, the use of standard CMOS surface morphology (Fig. 3) provides immediate fine pitch post-process capability.

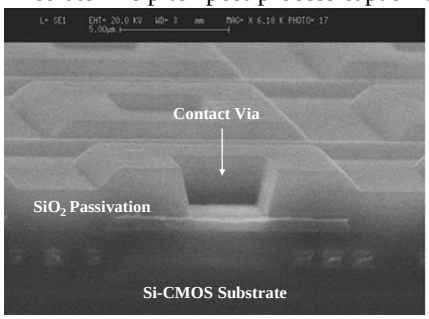


Fig. 3 Typical Si-CMOS Surface Morphology

Mask-less technology to build the UBM with a "Gap-fill" process

First, a UBM tri-metal stacked layer is full sheet sputtered (Fig. 4a). A planarizing resist layer is spin-coated on wafers to fill the vias. The resist is etched by an anisotropic O2 plasma (RIE) and the end of etch is controlled by the resist's thickness between the vias (Fig. 4b). The vias are protected by the resist and the unprotected top surface metal layers may be etched by a wet or dry etching (Fig. 4 c). The resist is then stripped to make isolated vias filled with UBM.

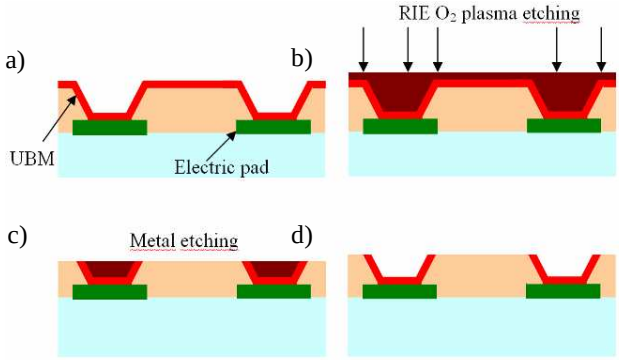


Fig. 4 Maskless "Gap-fill" process to make isolated UBM

Results on Gap fill UBM

Fig. 5a is a SEM picture of 10 µm pitch vias coated with a Ti/Pt UBM and ion-milling etched using the mask-less "gap fill" process. The metal over-etch showed on Fig. 5b is due to the resist over-etch during RIE O_2 plasma etching step. Indeed, in order to control the uniformity of the resist etching, an over etch has to be done. On 2000x2000 unplanarized vias with 10µm pitch, the maximum over-etch is around 650nm (measured by high resolution profilometer) on a passivation thickness of 2200 nm. However, better results can easily be achieved on planarized topology.

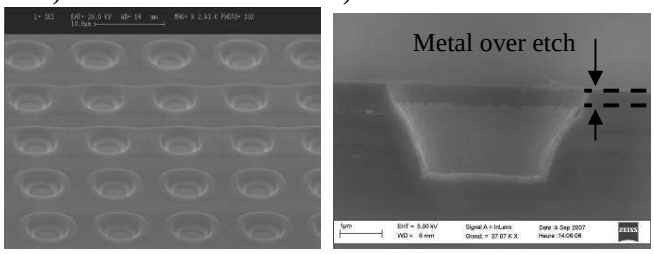


Fig. 5 SEM images of mask-less "gap fill" process to keep the UBM into the vias using the natural topology of the CMOS: a) top view of unplanarized 10 µm pitch vias, b) cross section of planarized 15µm pitch vias

3.2 Bumps fabrication for reflow technology

This technique is a modified version of a standard reflow soldering technique. The 4 millions bumps at 10 µm pitch are fabricated by a standard lift-off technique, however (and as expected) the bumps height and uniformity are degraded for a 10 µm pitch (Fig. 6) compared to "state of the art" 15µm bumps pitch.

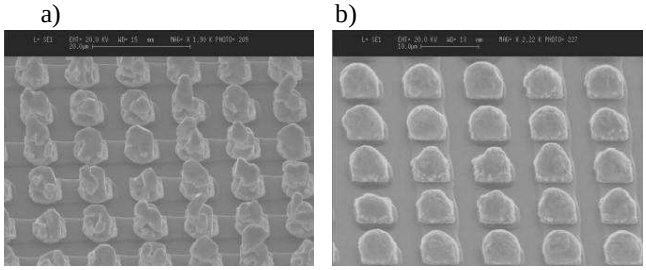


Fig. 6 SEM images of 10µm indium solder bumps made by lift-off technique: a) after lift-off, b) after reflow

3.3 Buried box fabrication for TB2 technology

Mask-less technology was also developed to fill vias (2,2 µm deep) with indium solder material. This technology consists in making a full sheet evaporation of indium (4,5 µm thickness) over UBM made by the mask-less "gap-fill" process. A widely accepted rule for planarization is to deposit a coating whose thickness is at least twice the depth of the vias, prior to polishing. Next, wafer is placed on a Logitech's jig and polished with Logitech® PM5 machine. The polishing planarity is both controlled by optical and mechanical methods. The pad used is made on extra-soft polyurethane (Chemocloth from Logitech®) and different powders (material, particule sizes repartition, shape) have been tested.

Best results were obtained with 1µm alumina powder and a pressure of 2,5KPa. The pressure parameter does not seem to critical for the homogeneity but rather governs the process. The polishing homogeneity is mostly governed by the materials under indium coating. Indeed, the adhesion of indium is lower over SiO_2 than over the UBM surface metal layer (most commonly gold or platinum). Therefore the indium wear rate is more important between vias (on SiO_2) than into the vias. Fig. 7 shows the results of indium polishing.

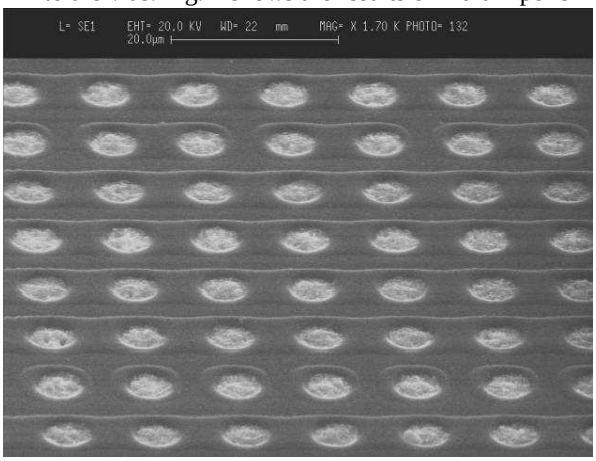


Fig. 7 2000x2000 vias with 10 µm pitch fill with indium solder material polishing on CMOS topology

AFM analysis has been done on 2000x2000 array with 7,5 µm pitch. A maximum dishing was measured around 550nm for a thickness of 2200 nm.

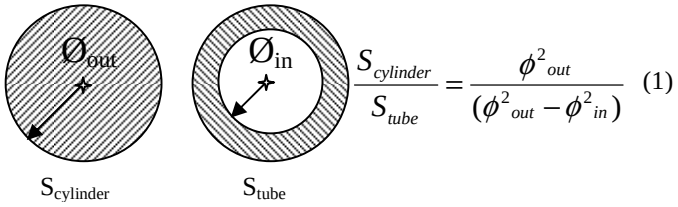
3.4 Fabrication of the micro-tips for reflow and TB2 technologies

Rational

In this study, all tested flip-chip technologies need micro-tips for hybridization (Fig. 2a and 2b). The development of a unique "tube shaped tips" process (patent pending) was chosen for all flip-chip sketches.

The insertion force is expected to be proportional to the inserted area cross-section of the tip in the TB2 technology. To reduce insertion forces we developed a proprietary process to make metallic micro-tubes.

The fraction between the surface contact of a cylinder and a tube is given by (1):



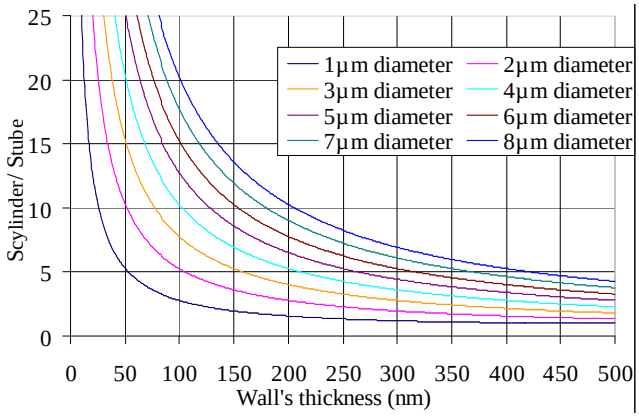


Fig. 8 Tabulated fraction between the surface contact of a cylinder and a tube

In the case of TB2 technology, the tube shaping:

-Minimizes the insertion surface by reducing the inserted tip area, hence the hybridization insertion force

-Increases lateral contact surface, hence decreases contact serial resistance

The process developed for such tube like structures uses conformal metal deposits and "gap fill" processes similar to those presented in the UBM fabrication section.

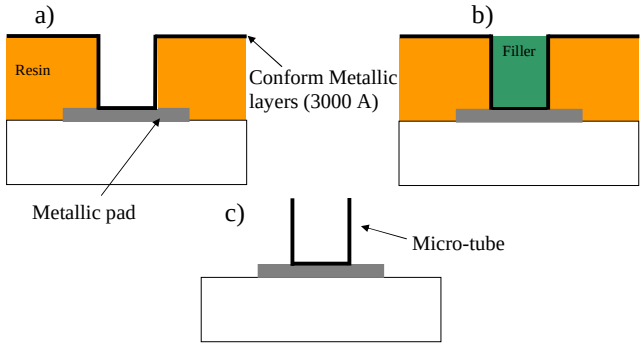


Fig. 9 Micro-tube process flow

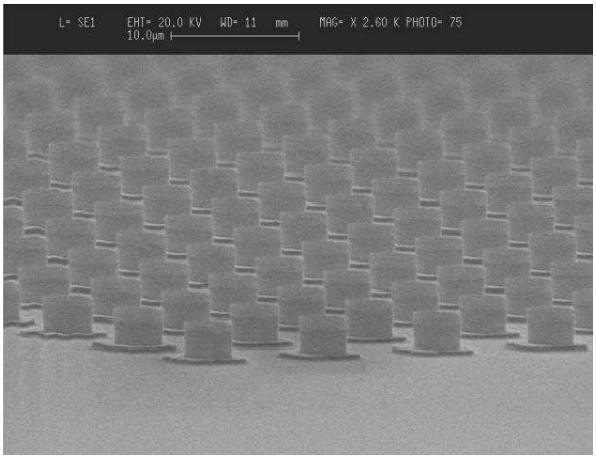
A polymer is first spin-deposited and photo-lithographed over contact pads. Metallic layers of 300 nm total thickness are then deposited (Fig. 9 a). A gap fill process is used to protect the metal located inside vias (Fig. 9b). Top unprotected metal layer is etched by RIE plasma and polymer removed by plasma cleaning thus leaving metallic micro-tubes on the wafer top surface (Fig 9 c). The height and the diameter of the micro-cylinder are defined by the initial polymer thickness and the photolithographic step.

Process was optimized on 3µm diameter micro-cylinder. Test patterns with 1 to 8 µm tube diameters were fabricated for full process capability evaluation.

Tube fabrication results

Arrays of 4-million micro-tubes with 10µm pitch have been processed with excellent yield and uniformity. Fig. 10 shows different micro-tubes diameters, between 2.5-2.8 µm height, aligned on metallic pad of 6x6µm². Micro-tubes from 2 to 8µm came out easily and simultaneously on the same wafer but 1µm diameter test pattern did not. This shows that specific process arrangements need to be developed to get down to such dimension.

a)



b) c)

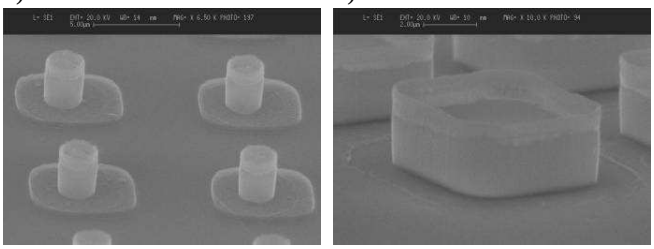


Fig. 10 Micro-tubes of a) 3µm diameter b) 2µm diameter c) 8 µm

The total metallic wall thickness of the deposited micro-tube is 300nm. However, due to the form factor, a wall thickness less than 300 nm was expected mostly for small diameters. From Fig. 11, the FIB image shows a wall thickness close to 100nm for 3µm diameter micro-tube. We can also see that the tip of the micro-tube is very thin and will be an advantage to decrease the insertion pressure. Notice that local in situ TEOS coating was deposited on the micro-tube to prevent any parasitic redeposit during FIB and improve the resolution of the measure.

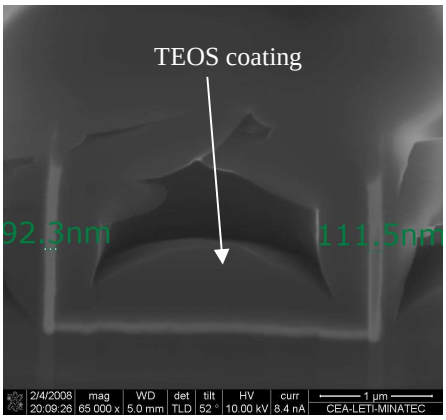


Fig. 11 FIB image of 3µm diameter micro-tube

3.5 Flip chip: reflow soldering technology

The bondings were done using a SET FC150 ® bonder with 500x500 interconnections with 10 µm pitch. A standard reflow soldering flip-chip technology was used, the only difference with classical process being the micro-tube tube presence instead of more conventional planar UBM soldering pads.

a) b)

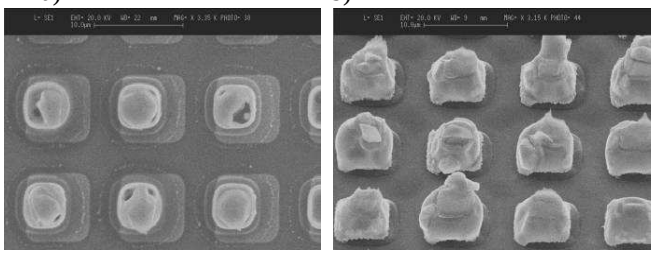


Fig. 12 FIB SEM images after pull tests of: a) micro-tube of 4 µm diameter at 10 µm pitch, b) indium bumps at 10 µm pitch

From Fig. 12 we can see both surfaces after pull out test. Gold finished micro-tubes show indium in their centers (Fig. 12a) transferred from bumps (Fig. 12b) meaning a solder joint was readily achieved.

3.6 Flip-chip: TB2 technology

Process characterization using micro-tubes array insertion in full sheet solder

The aim of this preparation study was to quantify the force per tip necessary for full penetration of a 500x500 micro-tubes array into a full sheet evaporated indium layer (6µm thickness). Three forces of 0.32; 1; 2 mN / µtube are used to make the insertion, then the top chip is disassembled and the required pull force measured. These tests were done on a Dage microtester 22.

As no metallurgic reaction is expected between the micro-tube's metals and indium solder, we assume that the pull force measured during disassembly is mainly related to friction force between indium solder and inserted micro-tubes.

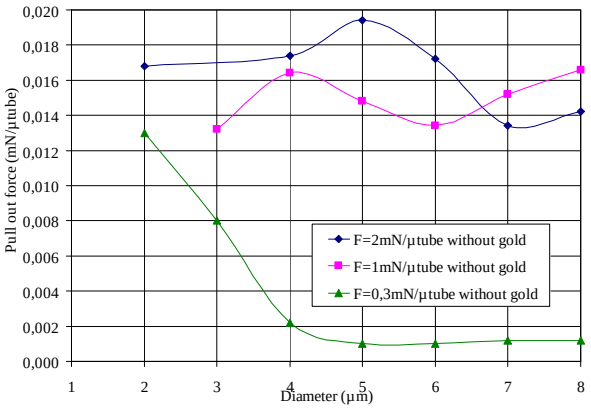


Fig. 13 Release pull out force of 500x500 micro-tubes inserted into indium sheet for different insertion forces and micro-tubes diameters

For insertion force of 1 mN/tube and 2 mN/tube, high pull force are measured which proves that the micro-tube are well inserted regardless of the diameter. This full insertion of micro-tubes is illustrated Fig. 14.

For insertion forces of 0.32 mN / tube, very low pull forces are measured for tubes diameter >4 µm (poor insertion), pull force increases dramatically for 3 and 2 µm tubes diameter. Better insertion can be explained quite thoroughly when considering tube perimeter and tube's wall thickness. Indeed, these parameters decrease with tube diameters (asserted by SEM measurements, see example on fig 11) and the insertion surface decrease too.

A first conclusion is that a minimum insertion force to fully insert micro-tube is included in the range [0.32-1] mN/µtube depending on tube diameter and tubes wall thickness.

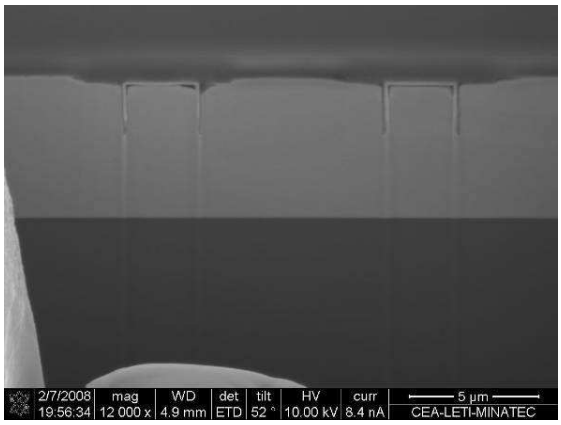


Fig. 14 FIB image of micro-tubes inserted at a pressure of 2mN/micro-tube into 6µm evaporated indium solder

Pull out forces are close to be divided by 100 folds compare to the insertion force for all diameters. To improve cohesive strength, a solution consists of creating a strong mechanical link between the tip and the solder by creating post-insertion low temperature $AuIn_2$ intermetallics [5].

Hence, in the next experiment micro-tubes were coated by Ti (400A) / Au (500A) sputtering. Insertions of 500x500 gold finished micro-tubes with 10µm pitch were performed with 0.3 mN/tube on all diameter range. A 5 hours / 80°C annealing was added to initiate a gold/indium (solid/solid) diffusion and the formation of an $AuIn_2$ intermetallic consolidation phase between tip surface and solder. [5]

From Fig. 15 the pull out force of gold finished micro-tubes with 5h/80°C increases for low diameters tubes (2 to 5µm) but not significantly for other diameters.

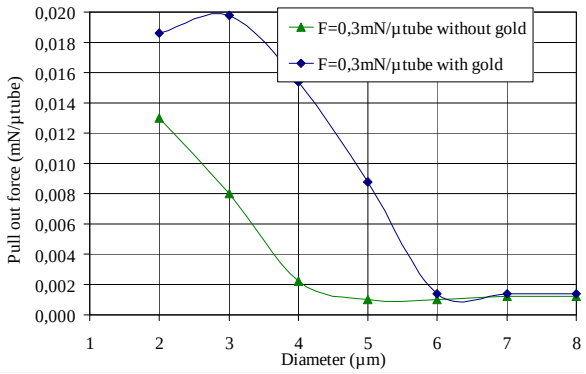


Fig. 15 Pull out force after 5h at 80°C annealing of 500x500 micro-tubes gold finished into indium solder material for different diameters (insertion force: 0.3 mN/tube)

Poor improvements of the pull out force between uncoated and gold finished micro-tubes for diameter above 5 µm are mostly related to poor insertion depth. As demonstrated before insertions of micro-tubes above 5 µm diameter are only superficial (Fig. 13). In this case, the gold to solder contact surface is too small to complete intermetallic phases and to reinforce cohesive mechanical properties.

However, SEM images of the 3 µm diameter gold finished micro-tube prints, after pull test, show some missing indium solder region meaning an intermetallic consolidation (Fig. 16).

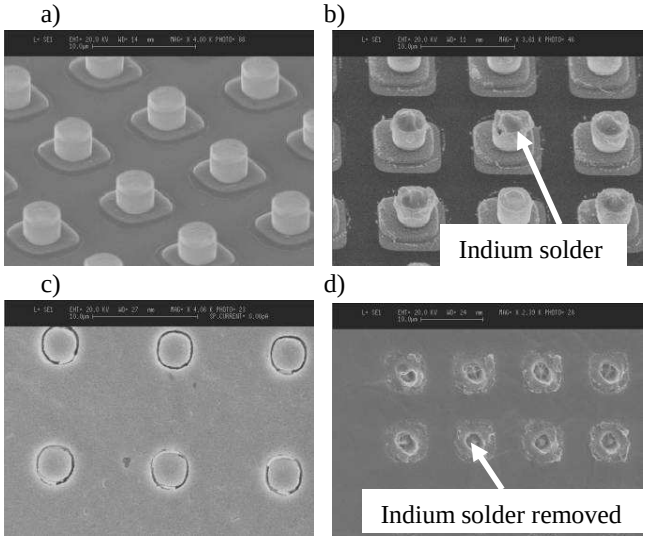


Fig. 16 SEM images after pull test of: a) 3µm diameter uncoated micro-tubes, b) 3µm diameter gold finished micro-tubes with 5h/80°C, c) 3µm diameter uncoated micro-tube prints into indium full sheet solder with 5h/80°C diffusion step, d) 3µm diameter gold finished micro-tube prints into indium full sheet solder with 5h/80°C diffusion step

The pull out results for the gold finished micro-tubes results were not as good as expected which is probably due to a too thin gold thickness.

The drawback of pull test is the separation mode of the two dies. Indeed it may not correspond to a simultaneous separation of all the micro-tubes of the upper die from their indium target. It can rather correspond to a complex peeling mode and the calculated mean pull out force per micro-tube is certainly underestimated. Moreover pull out test does not give a direct access to the load/displacement micro-tube curves.

Process characterization using nanoindenter and single tip insertion

To obtain more accurate insight into the tube insertion process, a nanoindentation apparatus (MTS instrument, nanoXP) was modified. Isolated 13µm radius indium bump reflowed on 3x3 mm^2 silicon chip (Fig. 17) were mounted at the end of the indentation column facing 5x5 mm^2 dies with 500x500 micro-tubes of 3µm diameter and 2.8 µm height at 10 µm pitch where mounted on the substrate holder as target to the indium bumps.

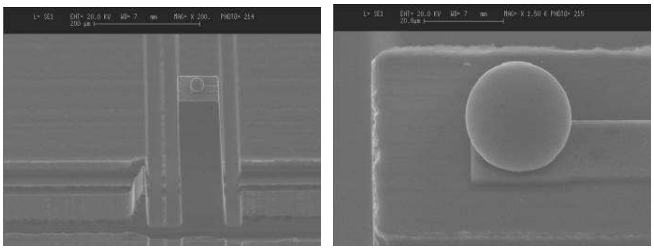


Fig. 17 Sample of 26µm diameter indium solder bump over 200µm silicon structure for unitary insertion by a micro-tube

In this configuration, four insertion experiments were carried out. Each experiment corresponds to one new indium bump and one new micro-tube.

Insertion experiment number	1	2	3	4
Tube gold coated	no	no	yes	yes
Target die number	1	1	2	2
Loading rate (µN / sec)	33.3	33.3	33.3	33.3
Max load (µN)	1382	295	1043	575
Creep delay (sec)	240	240	240	240
Load decrease during creep (µN / sec)	81	26	71	45
Unloading rate (µN / sec)	33.3	33.3	33.3	33.3

Table. 1 Single tube microinsertion experiment parameters

Indium bump versus micro-tube axis alignment is performed with a +/- 1µm lateral precision using the indenter column as a profilometer. During this operation, contact force between the micro-tubes and the indium bump is always bellow 3µN. Insertion tests are constructed to simulate the matrix die assembly process with a 2 mN/min loading and unloading rate and a 4 minutes creeping stage at max load. Max Load for experiments 1 and 3 are not explicitly chosen at the beginning of the experiment but is automatically chosen during the experiment to correspond to a 3.5 µm insertion depth to be sure to have a contact between indium top surface and tube bottom. Maximum load for the experiments 2 and 4 was explicitly chosen to have indium surface just in contact with tube bottom after analysis of experiments 1 and 3 results.

After the experiments, each indium bumps was observed with a SEM (Fig. 18). Experiment 1 SEM image shows a slight imprint of the tube at the bump top due to a too high tube detection load level at the beginning of the experiment. We consider that it has not impacted the obtained load vs. displacement curve.

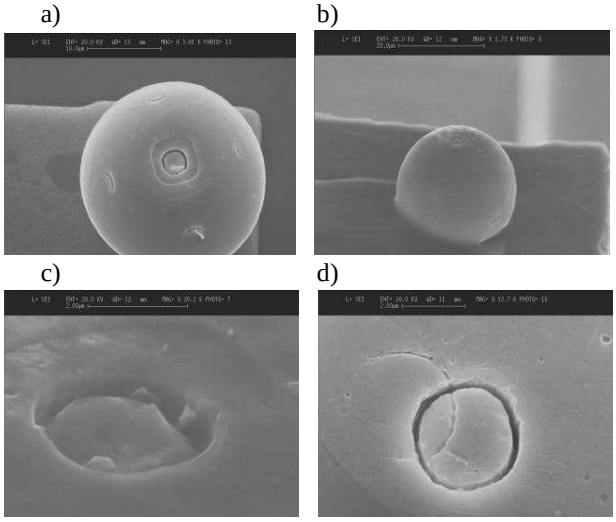
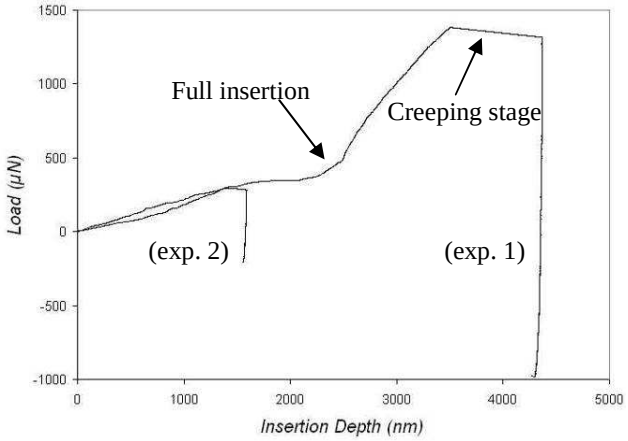


Fig. 18 SEM images of indium bumps after experiment : a) experiment 3, b) experiment 4, c) experiment 4 detail, d) experiment 1 detail

Fig. 19 shows the obtained load vs. displacement curves for respectively the two uncoated and the two gold coated micro-tubes at different loads. Main results of the experiments are described in Table 2. In both cases, indium contact with tube bottom is identifiable on the displacement curves at roughly 2.6 µm depth by a change of the curve slope which is confirmed by the SEM images of indium bumps (Fig. 18) where the impression mark of the rectangular metallic pad positioned under the tube bottom can be identified. Simple geometrical consideration shows that at 2,8 µm insertion depth, the first neighbours of the tested tubes should also touch the indium bump surface as seen on Fig. 18a. Only experiment 2 didn't insert the tube down to it bottom. Full micro-tube insertion arise at loads around 500 µN and no appreciable differences is seen between gold coated and uncoated tubes. At maximum load, the 240 seconds creep time corresponds to the plateau on the curves. This plateau is slightly decreasing due to applied load drift. The obtained drift values during experiment are summarized in table 1. Creep depth is important and corresponds to tube insertion at

constant load for experiment 2 and bump flattening for the three other experiments. Tubes pull out occurs without important tube breaking as shown with SEM images of tube imprints (Fig. 18). Pull out occurs suddenly when a critical pull out load is reached. Assembly elongation is of tens of nanometers. The higher the maximum load applied, the higher the tube pull out load, with a pull out load that should be situated between 200 and 500 µN for a tube ideally inserted with the indium surface just touching the tube bottom.

a)



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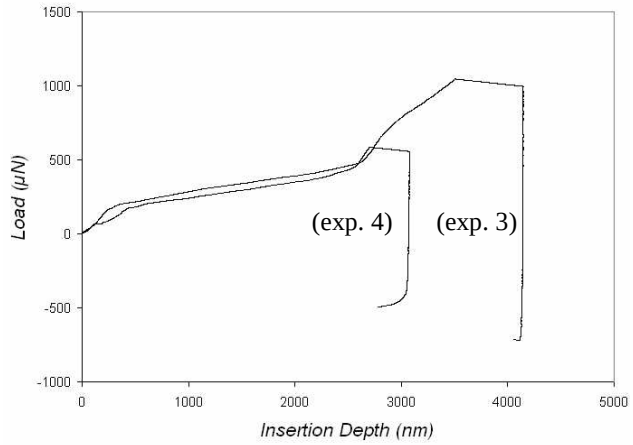

Fig. 19 Load vs displacement curves for insertion experiment: a) uncoated tubes (exp. 1 and 2), b) gold coated tubes (exp. 3 and 4)

	1	2	3	4
Load at indium contact with bottom (µN)	490	n.p	510	478
Creep plateau depth (nm)	835	185	612	349
Pull out load (µN)	-980	-212	-719	-492
Pull out assembly elongation (nm)	70	33	43	50

Table. 2 Single tube microinsertion experiment results

Finally, pull out curves does not help concluding on a different behavior of gold coated and uncoated tubes. The only noticeable difference arise on the first 200 µN of loading where tube insertion is more difficult for gold coated tubes certainly due to their less sharp wall at the top.

Using the nominal hardness value of 8,8 Mpa [7] for indium, the plastic deformation should begin at 8,3 µN for ideal 200 nm thick tubes. Therefore, we can consider that load vs. displacement curves correspond mainly to viscoplastic deformation of indium and further analysis of insertion mechanism will require the study of insertion creep behaviour of micro-tubes under constant load and at different insertion depth.

Comparison between area array insertion and single tip pull out tests on 3 µm diameter micro-tube

		Insertion force (µN/µtube)	Pull out force (µN/µtube)
Area array insertion	Uncoated	[320 ; 1000]	> 8
	Gold coated		> 20
Single tip insertion	Uncoated	≈ 500	< 210
	Gold coated		490

Table. 3 A summary of main insertion results from both techniques (nanoindentation & pull out tests) on 3 µm diameter micro-tube

Minimum single tip insertion force is measured to be 500 µN which is effectively inside the initial range of [320 ; 1000] µN indicated by area array insertion method.

Single tip pull out forces are much higher than those calculated with area array method. This indicates that a complex peeling mode is taking place during the separation of the 500x500 array connections.

Considering a 500 µN single tip insertion force, calculated insertion force for 4 megapixels area array should be 2 kN, which is easily achievable with SET FC300 ® flip-chip bonder.

4. Next steps

Previous results show that the insertion forces are proportional to the micro-tube diameters. Next the hybridization of 4 megapixels arrays will be achieved using 3 to 5 µm micro-tube diameters which are the available tubes today.

The next following step will be to investigate the newly developed reflow soldering and TB2 techniques using available (ready for flip-chip) 4 megapixels arrays. Indeed, to test electrical performances of the bonding techniques daisy chains have been implemented on chips (Fig. 20) to accurately calculate the resistance access and the defectivity (open or short circuits).

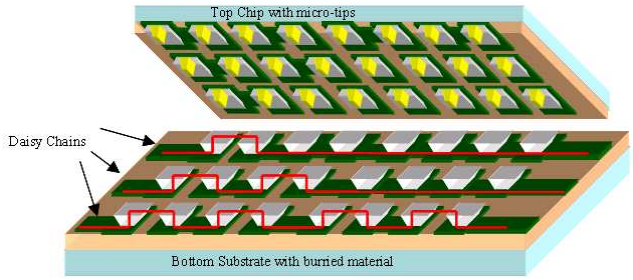

Fig. 20 Daisy Chain Test Vehicle for Electrical Validation

Both bonding types (reflow or thermocompression) between chips will be done using the SET FC300 ® bonder thanks to its reflow soldering or thermocompression versatile configurations. The alignment capability of the bonder is a primordial parameter and the misalignment of this equipment should be less than ± 0,5 µm at the 2 kN thermocompression force required in our case.

Eventually, reflow soldering can be achieved using oxyde reduction atmosphere or vacuum to avoid gas trapping inside tubes.

Different annealing and gold thickness will be performed to improve pull out forces and electrical results. More experiments should be done on unitary tip insertion by nanoindentation to optimize the insertion process. Indeed, creep delays must be studied to further decrease the insertion pressure.

4. Conclusion

The latest developments on technologies for high complexity 10 µm pitch area arrays hybridization have been presented. Important efforts were done to modify the buried box fabrication from CMOS vias in a maskless and low cost process at 10µm pitch. To reduce insertion force, a proprietary process to build 4 million metallic micro-tubes with 10 µm pitch has been developed. Insertion pressure has been theoretically reduced by 8 folds for a 3 µm diameter micro-tube compared to a full cylinder tip. A unitary insertion experiment was used to measure the minimal insertion load, which was up scale to estimate the load for a 4 million area arrays hybridization.

Next step will be to measure electrical resistance of such interconnections made by reflow soldering and thermocompression and choose which should be the best scalable technology for future.

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