Ultrathin 3D ACA FlipChip-in-Flex Technology

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Abstract

Die thickness of common, high-volume chip stacks range between 50-100 µm while thinning industry aims towards ultrathin chips of 10 µm thickness or even below. For the first time, the required interconnect length between vertically arranged adjacent chip layers has therewith reached dimensions, that can be reasonably realized by anisotropic conductive adhesives layers (ACA). Accordingly, a three dimensional arrangement by alternate stacking of ultra thin flip chips and interposers using anisotropic conductive adhesive bonding technology is within the bounds of possibility, such that the conductive particles are forming the vertical interconnects between the chip-interposer layers.

Based upon such assembly concept prototypes have been made within a first laboratory scale feasibility study. In combination with polyimide thin film interposers, ultrathin low pin count ACA bonded test chips with 4-Point-Kelvin- and Daisy-Chain-structures have been used to build a 4-layer flip chip stack with a thickness of approximately 170 µm without encapsulation. First electrical measurements have shown promising results.

The reduction to basically one bonding technology to realize the chip-interposer- and the interposer-interposer connections is one of the main benefits with a certain low-cost potential. On the other hand, issues as limited chip/package area ratio, the demand for ultrathin chips with manifold challenges and upcoming detailed electrical characterization of such chip stacks have to be considered. Pros and cons are openly discussed.

Special attraction is provided by applying and combining basically known packaging technologies to obtain an innovative but somehow simple 3D flip chip assembly with certain future application potential.

1. Introduction

Electronic products as cell phones, PDAs, digital cameras and other consumer products follow the overall trend of maximum functional integration in the smallest package and lowest packaging costs. Here, 3D-packaging is one of the key issues to achieve these goals. On chip integration level several stacking technologies exist. Among those die-stacking in combination with wirebond technology still plays the most prominent role [1].

Developments have lately been made with various embedding technologies, such as Chip-In-Polymer [2, 3] or Chip-In-Substrate [4], that are mainly based on PCB-compatible processes having a certain low-cost potential. Higher integration levels are achieved with wafer-level-processes at which most R&D is concentrated on Through-Silicon-Vias (TSV). Nevertheless, several groups are working on other promising 3D-chip integration technologies on wafer level [5, 6].

Among performance and cost issues, more or less, most of the technologies focus on the smallest footprint or chip/package area ratio and the lowest profile. Further reduction of the required area is somehow limited by the minimum chip area and hence beyond packaging issues. In fact, wafer thinning is one of the key wafer back-end processes for further reduction of the package height as being one of the primary issues of many developments [7, 8, 9]. Die thickness of common, high-volume chip stacks range between 50-100 µm, but thinning industry aims towards ultrathin chips of 10 µm thickness or even below [10]. Albeit current possible handling, performance and cost issues, that arise from packaging of ultra thin chips, those dimensions open up the development of new stacking technologies.

The basic idea for the described stacking concept has been derived from the basic fundamentals gathered from several projects dealing with handling, assembly and reliability of thin chips and thin interconnects. Here, mainly anisotropic conductive adhesives (ACAs) and thermode soldering processes have been evaluated and compared [11]. Among several advantages such as low cost and fine pitch capability, ACAs have been found having good reliability [12]. Hence, it is widely used not only for display packaging (chip-on-glass, COG) but also for chip-on-flex (COF) and chip-on-board (COB). ACA has the potential for low and ultra low profile FC-assemblies due to the availability of thin and ultrathin chips and substrates in combination with thin and ultrathin metal layers such as thin bumps or UBMs (under bump metallizations) only and thin substrate pads. By using thin chips (< 50 µm) contact thickness significantly contributes to the total thickness of a flip chip assembly. Thus, ultra-low profile FC-assemblies of appx. 20 µm height or even below are within the realms of possibility. For the first time, the required interconnect length between vertically arranged adjacent chip layers has therewith reached dimensions, that can be reasonably realized by anisotropic conductive adhesives layers (ACA) as described below.

2. Concept

The basic stacking concept is schematically illustrated in figure 1 [13].

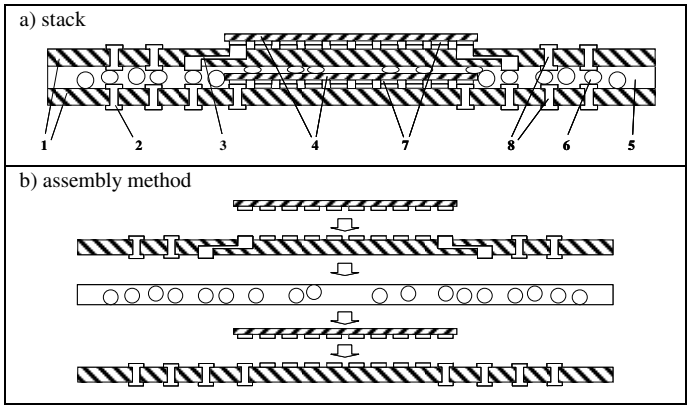


Figure 1: stacking concept and assembly order

It is mainly characterized by an alternate stacking sequence of substrates or interposers (1), Flip Chips (4) with interconnects (7) and ACA layers (5) including conductive particles (6). The interposers are double sided substrates with metal layers on both sides (2), vias (8) and at least one internal wiring layer (3). Figure 1b) shows a possible assembly order of the components. On a first base interposer a first chip is mounted with any flip chip technology. A second interposer is then large-area bonded with anisotropic conductive adhesive onto the first chip-interposer module. Flip chip assembly of a second chip with any kind of flip chip technology follows, such that a chip stack including the minimum number of two ICs, is realized. Other levels may follow to raise the number of chips. The vertical interconnections between the levels are realized by anisotropic conductive adhesive and the interposer vias including pad metallizations (z-axis). User-defined routing of the chip I/Os is possible due to manifold interposer layout options (x-, y-, z-axis). This stacking concept mainly benefits from an ultra low flip chip profile (except for the top level), such that the vertical distance between the interposer levels may mechanically and electrically mostly be bridged by anisotropic conductive adhesive, respectively electrically conductive particles. The minimum size of the conductive particles is selected, such that a typical ACA interconnection, providing electrical and mechanical interconnection, between the interposers is reached. The possible minimum size of the particles depends upon the flip chip assembly thickness as well as from the thickness of the bottom metallizations of the next level interposer. The latter may contribute to bridge the gap up to a certain extent as long as similar structures directly above the chip in the lower level are avoided. In this case, the necessary particle diameter may be beneficially reduced in terms of a higher pad density or pitch reduction. However, in this regard, thickness of the top metallizations of the interposer of the lower level is irrelevant, if all pads, including flip chip pads, have the same thickness.

Preferably, compliant particles should be used to allow for sufficient deformation especially in the center area, where the chips are located. Here, in comparison with the periphery, the gap is reduced about the degree of the flip chip assembly height, resulting in a higher necessary degree of particle deformation in case of compliant particles. Undeformable particles are expected to damage the chip or/and next level interposer as long as a certain flip chip assembly thickness can not be avoided. The necessary particle deformation degree depends upon the ratio of the particle diameter and the flip chip assembly thickness, such that a lower ratio requires a higher deformation degree, considering that the thickness of the bottom metallizations of the next level interposer can be neglected.

Due to the ultra low height of the flip chip assembly large-area application of ACA across the overall module including the flip chip is possible.

The ACA additionally provides a certain chip embedding as well as spacer functionality, keeping the interposers within the necessary distance. Both mean an expansion of the previously used benefits of ACA.

Basically, the technology is not limited to a certain maximum thickness of the internal flip chip assembly, but in terms of reasonable peripheral interconnection pitch between the interposer levels, its application requires a certain minimum thinness. Lower flip chip profiles permits the reduction of the size (diameter) of the electrically conductive particles, which, in turn, directly increases the possible peripheral interconnection density, decreasing the minimum interconnection pitch, respectively. Total flip chip assembly thicknesses of 20 - 50 µm are the estimated reasonable maximum limit for the majority of possible applications. Additionally, matched pad thicknesses, as mentioned above, may contribute to obtain higher interconnection densities between the interposer levels.

Certain attraction is provided by the fact, that the main assembly process can be reduced to a sequence of flip chip processes of the same type. So, once good chips and interposers are selected, the main task is to optimize the flip chip processes up to a sufficient yield.

Within a first experimental approach the feasibility of such stacking concept has been investigated

3. Experimental

3.1. Layouts

Stack Layout

The complete chip stack consists of a total number of four ICs (test chips 5 x 5 mm^2) and four PI-interposer fan-out levels (10 x 10 mm^2), which are alternately stacked (figure 2).

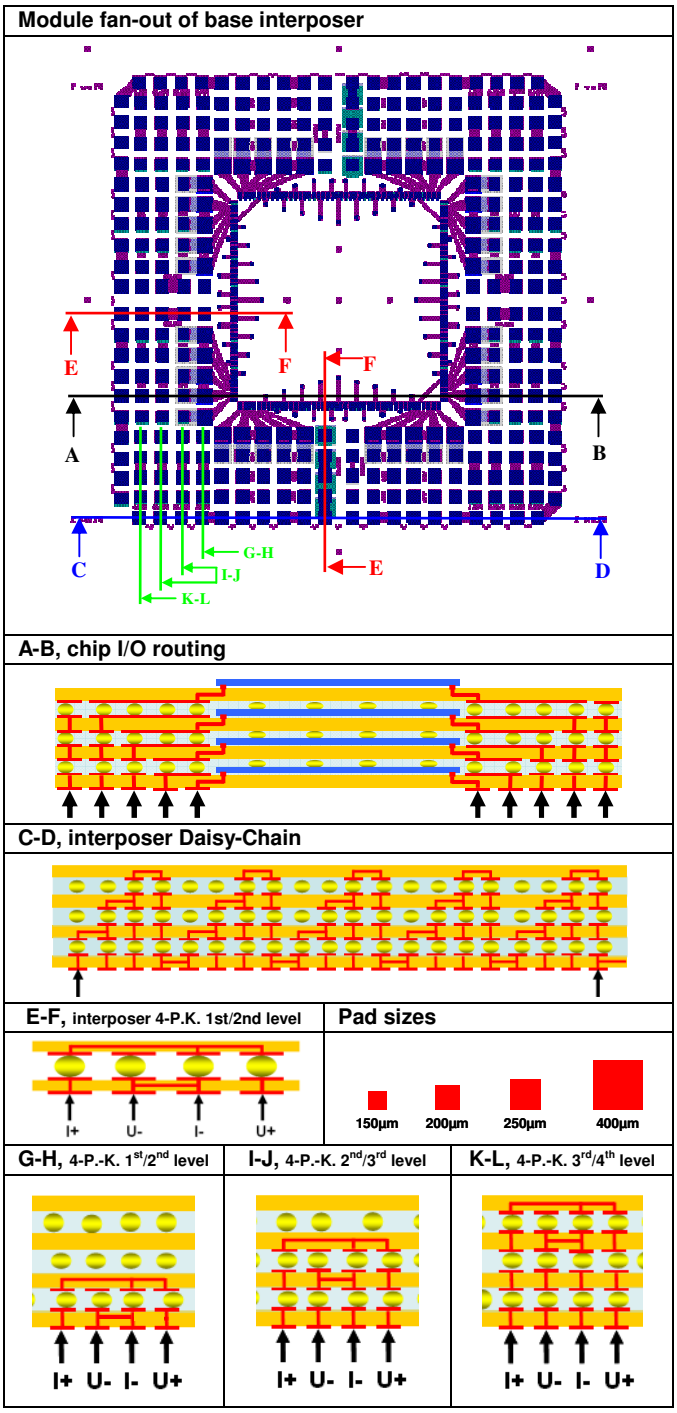


Figure 2: stack layout

The layout is designed, such that the electrical access is exclusively gained from the bottom pads of the first base interposer. Each chip can individually be measured which means, that all necessary I/Os (40 each chip) are separately routed (Figure 2, A-B). To a certain extent, this allows for a pad enlargement between adjacent interposer levels. Although this is not considered absolutely necessary, it may improve the electrical contact (DC) due to a higher number of trapped particles. Successful measuring of the chip interconnects (4-Point, Daisy-Chain) certainly requires adequate operation of the necessary vertical interconnects down to the base level. Additionally, there are several test structures to characterize the interposer interconnects separately. This includes a stepped circumferential Daisy-Chain which is located at the edges of the module (Figure 2, C-D) as well as several 4-point-Kelvin structures. One each of such structures is peripherally arranged at the edges of each quadrants (Figure 2, E-F), whereas two of the total eight structures have the same pad sizes each. Lengths of the pad edges are 150, 200, 250 and 400 µm. Hence, the contact resistivity between the 1st (base) and the 2nd interposer can be measured. Additionally, similar test structures, all having identical pad sizes (250 µm edge length), are located in the corners of each quadrant to detect the contact resistivity between the 1st and 2nd (G-H), 2nd and 3rd (I-J) as well as between the 3rd and 4th (K-L) interposer levels. As well, to gain electrical access to the advised structures in the upper interposer levels, functional interconnections between the involved lower levels are required. A total number of 76 test structures can be measured, requiring ca. 520 interconnects between interposers 1-4.

Interposers/Substrates

Each of the four interposers consists of three layers of polyimide and comprises electroplated Au vias between two-level metallisation of sputtered Au. This is the minimum number of layers necessary for the realization of the test patterns. Most of the chip stacking applications will get along with only one metal layer, considering the 2nd metal layer only necessary for the specific interposer characterizing 4-Point test patterns with overlapping conductor lines. Due to cost savings, here, the design of all four interposer levels has been arranged on one wafer (one set of masks only). The total thickness of the substrate is around 12 µm, 5 µm of polyimide for the first and third layer and 2 µm for the layer in between. The metal line thickness is in the range of 100 to 300 nm, in order to keep the high flexibility of the substrate. Although this is not considered necessary for the present stacking technology, it expands the broad range of possible applications of such substrates. Thicker metallizations are possible if needed. Deformation analyses were performed to evaluate the grade of plastic deformation depending on bending radius for different materials and thicknesses. The minimum aperture width in a 5 µm thick polyimide layer is around 10 µm, the lines and spaces of the metal lines can be in the range of 1 or 2 µm, depending on the lithography limitations. Due to the substrate application, line width and spacing of a few tens of microns is used (min. 50 µm lines/space). The process steps are graphically illustrated in figure 3.

The polymide used here is non-photodefinable, so the layers are patterned by dry etching. The advantage is the low shrinkage, the lack of photo initiators and the minimum feature size, which can be achieved by dry-etching. The foil interposers are manufactured on a temporary wafer substrate and later released. As the approach for plating bases on electroplating from the bottom of a mould, the manufacturing starts with a seed layer for plating. Due to this approach, the design needs to care for a continuous path of a line to a mould to be plated. The following process is an iterating sequence of PI application (SpinOn, Dry, Dry etching), via-formation (Au plating) and Au sputtering (metallization), such that each interposer is realized in accordance with the stack layout.

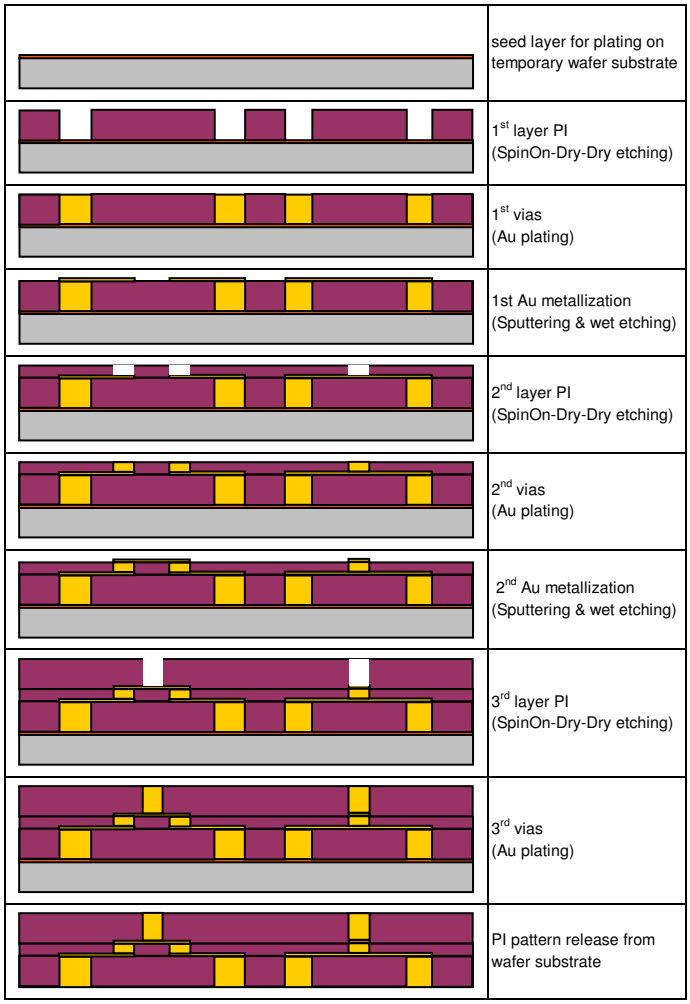


Figure 3: thin film process steps

Before sputtering, depending on the application, adhesion layers like Ti or Cr maybe used, but not preferred as this results in extra efforts for patterning the lines. A pre-treatment of the surface normally is sufficient for meeting adhesion requirements. The metal lines are patterned by wet etching the sputtered Au. A special Au etch can be used, for least undercut in case of minimum pitch requirements. If pitch is not critical, iodine-based solutions may be used. If adhesion layers are employed, etching solutions need to be used, which yield least undercut in combination with Au. Least undercut in the range of layer thickness can thus be achieved. Finally, the outer geometry of the substrate is defined in a photo resist mask and then dry etched again down to the initial seed layer. Finally, the polyimide patterns are released from the substrate. The design concept comprises supporting bars, which keep all patterns in the wafer configuration, which facilitates the handling in following steps. For separation of the individual devices, those supporting bars are removed by Laser or just cut out.

The major achievements in the manufacturing sequence are the fine-tuning and adoption of curing steps of each polyimide level, the plating of Au at low-stress and high grain stability in curing steps, fine pitch patterning of polyimide and metal lines, good adhesion of plated and sputtered metal, which also comes along with specific design approaches and rules. The most

important achievement is the adhesion and reliability of electrodes or pads for bonding applications. The specific design for bonding pads interlocks the polyimide layers between the plated material. In this concept, the pads are supported by at least one other plated pattern in the second polyimide level interlocking the pad in the first or third level of polyimide. This secures that the pad is not failing or falling out of the foil. If the pad is formed like a plated plug reaching through all of the three polyimide levels, mechanical impact on the foil and its integrity is very low.

ICs

Following chip test layout has been used:

- Silicon, 5 x 5 mm²,
- test patterns for electrical measurements of 4 Daisy-Chain and 8 Four-Point-Kelvin-structures,
- 176 I/Os total, 40 IOs used
- chip thickness 10 – 12 µm
- pitch 100 µm
- bump metallurgy 3 µm Ni(Au)

3.2 Technologies, Materials

Wafer bumping / thinning

Common bumps for ACA technology are either made by mechanical stud bump bonding [14] or various chemical deposition technologies, ranging from evaporation to plating processes. Here, electroless nickel deposition has been used, as it benefits from its low cost potential [15, 16]. The standard electroless nickel UBM for high reliability has a thickness of 5 µm but only a minimum of 1 µm is necessary to have a closed and void free nickel layer [17]. The used test chips had a final Ni(Au) thickness of 3 µm (Figure 4).

Wafer thinning to a final chip thickness of 10-12 µm has been made by an external supplier.

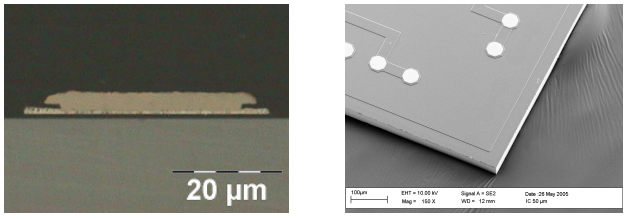


Figure 4: 3 µm Ni(Au) bump

ACA

To simplify the stacking process it is reasonable to choose ACA technology for both, the interposer as well as for the flip chip bonding steps. Nevertheless, flip chip bonding may also be performed with flip chip thermode solder processes, as well having potential for ultra thin interconnects [18]. In either case, due to bending and warping of thin and ultrathin ICs, minimum bonding forces have to be applied for planarity and interconnection issues. Adhesives are of paste or film form either. Two types of ACA have been used. For the flip chip assembly commercially available ACP has been used (3 µm Au coated polymer balls, ACA I). Bonding of the interposers requires the formulation of an ACA, such that the general conditions, as e.g. adequate particle size, compliance and snap cure properties, can be kept. The used ACA has been composed of commercially available NCP loaded with conductive particles. An ACA with Ni(Au) coated polymer balls, having a diameter of 30 µm, has been mixed, using standard mixing equipment (ACA II). This has been considered being a reasonable particle size, well adapted to the flip chip assembly thickness (figure 5) and the wiring density (lines/space: 250µm/200µm). Nevertheless, there is potential for further reduction of the particle diameter.

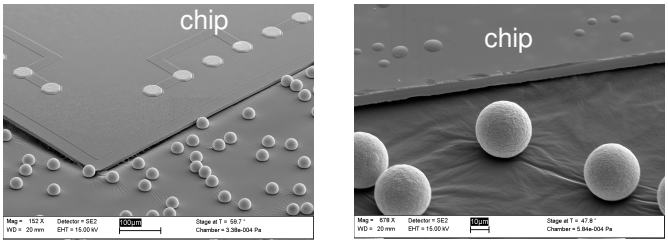
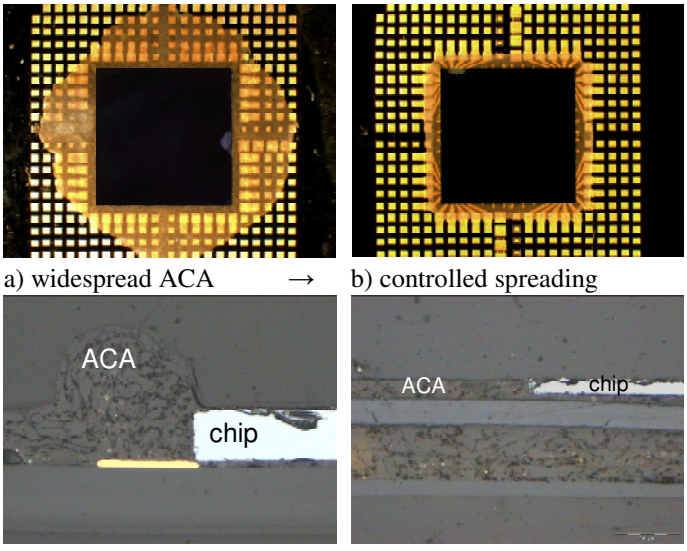


Figure 5: ACA particle size (30 µm) against chip thickness (10 µm)

Assembly

As mentioned above, the assembly process is an alternate stacking sequence of interposers and flip chips by using ACA technology, whereas the flip chip assembly basically poses the bigger challenge.

Generally, large-area application of ACA is done on the substrate or interposer respectively. The ACA bonding process requires a certain pressure to trap electrically conductive particles between the bumps and the substrate metallization to form an electrical contact. Applied heat on the bonding tool and chuck is needed to cure the adhesive. Here, ACP has been dispensed, followed by an optimized flip chip bonding process. Central demands include complete filling of the gap and marginal spreading of ACA beyond the chip edges (xyz). The former is mainly important to give sufficient mechanical support for the chip considering the following load (assembly) steps as well as to achieve necessary electrical contact. The latter corresponds to the basic need to prevent from wetting the nearby pad structures that are essential for the interconnections to the next interposer level and to keep an ultra low (flip chip-) profile (figure 6).



a) widespread ACA → b) controlled spreading

c) ACA z-axis overlap → d) ACA levelling

Figure 6: spreading of ACA

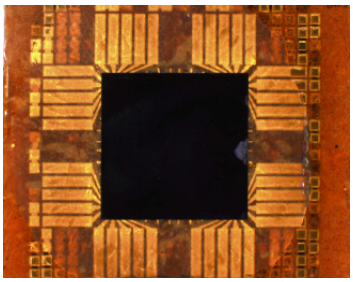
Accordingly, the tolerances of the ACA distribution are very low compared with standard ACA-technolgy. Controlled spreading of ACA, as shown in Figure 4b), is barely to achieve. This is mainly traced back to the fact of the ultra thin bondline below the chip (~10 µm), respectively the very small volume that needs to be filled with ACA. What's worse, spreading of ACA beyond the chip edges is even supported due to the

demand for a low profile across the entire plane (Figure 4d), such that formation of excessive ACA along z-axis (Figure 4c) must be prevented. Standard dispensing accuracy, especially minimum amount of adhesive in combination with complex flow properties of ACA, is beyond the present requirements. Use of common ACF (Anisotropic Conductive Film) is only little better than ACP, as it reveals slightly different but basically the same challenges. Controlled ACA distribution, using commercially available material, as shown in Figure 4b) has been achieved within a laboratory scale only. Use of a matched flip chip tool geometry lead to the necessary levelled ACA surface as depicted in Figure 4d). Currently, both issues are the bottlenecks, complicating the assembly of a higher number of modules. In this respect, the technology will definitively benefit from waverlevel-ACA as it is expected to have the potential for an optimized distribution of adhesive. First experiments have shown promising results (see also 4. Packaging Options). Nevertheless, prototypes of the described stacking technology have been assembled, whereas a single Flip Chip Bonder (*Suess Microtec FC150*) have been used. A total of seven assembly steps (4x flip chip, 3x interposer), each including an ACA dispensing step, are necessary for the complete formation of the package.

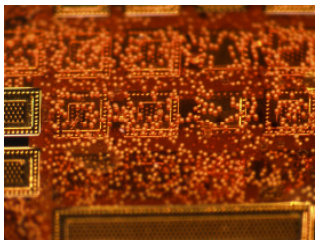
3.3 Results

Functionality

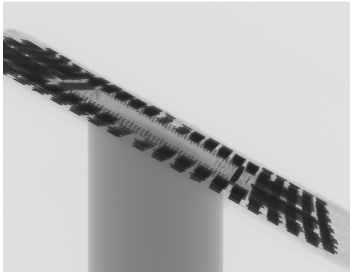
The top view of the complete module is shown in figure 7a).



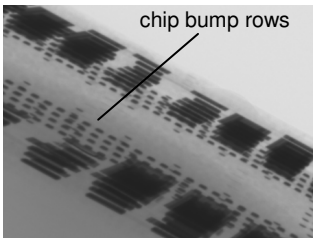
a) top view



b) detail



c) x-Ray/CT side view



d) detail x-Ray/CT side view

Figure 7: chip stack module

Widespread ACA from the last flip chip assembly (top level) is the reason for the partially matt-finished surface. Outside, due to the optical transparencies of the ultra thin interposers and adhesive layers, the lower interposer and ACA levels can be seen from the top up to a certain extent (figure 7b). The four chip levels are clearly indicated by the chip bump rows, made visible by x-Ray inspection (figure 7c),d).

Figure 8 contains the complete measurement data of one of the prototypes. After each assembly step (7 in total, from left to right) a set of measurements (framed blue) is added due to the stack layout. Hence, possible change of the electrical performance after each assembly step can be determined. Up to know, no statistics have been applied due to the low number of modules. The relatively large number of light green highlighted measurement structures after the 7th process step (framed dark green) indicates the predominant final electrical functionality of the test structures. Beyond a set of failed interconnects between the 1st and 2nd interposer (Flex I-II), only a few additional structures in the higher levels have failed (marked orange, 4-Point-Kelvin R > 500 mOhm). Even though, average values of passed test structures change in the course of the process, none of them significantly degrades or even fails. In fact, the chip 4-Point-Kelvin- and Daisy-Chain-resistivities stay relatively constant. The average final chip 4-Point resistivity ranges between ca. 60-275 mOhm whereas an increase from chip I to chip IV can be observed. The interposer test structures have shown a relatively constant average final 4-Point resistivity (equal pad length 250 µm) between ca. 15-170 mOhm (Flex I-II, Flex II-III, Flex III-IV). 7/8 of the stepped circumferential Daisy-Chain (Flex I-IV) is fully functional.

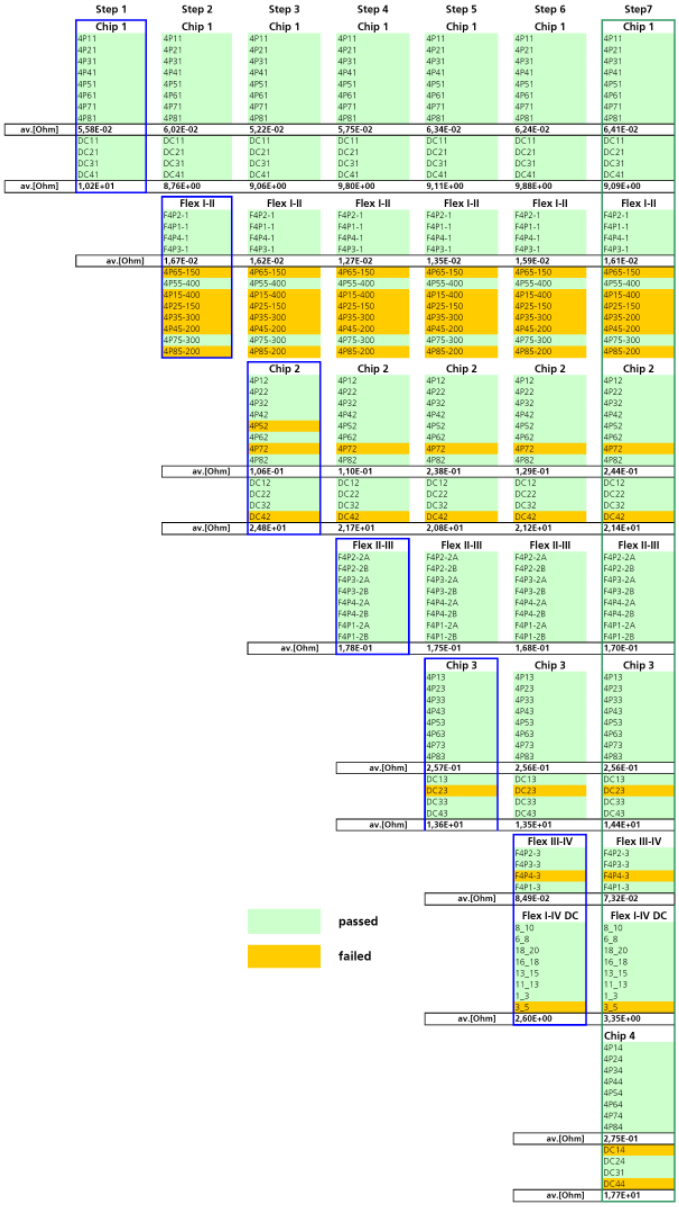
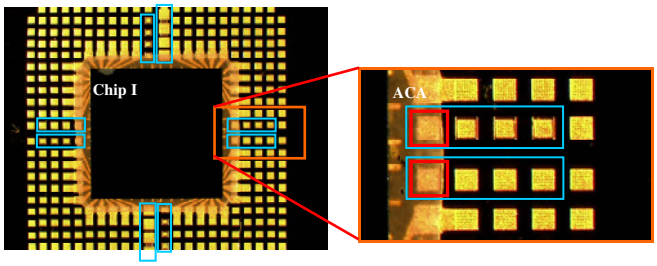


Figure 8: 4-layer stack, electrical data

After the final assembly step operation of >90% of the test structures has been achieved (2nd part of data of block "Flex I-II" reasonably excluded, also see *Analysis).*

Analysis

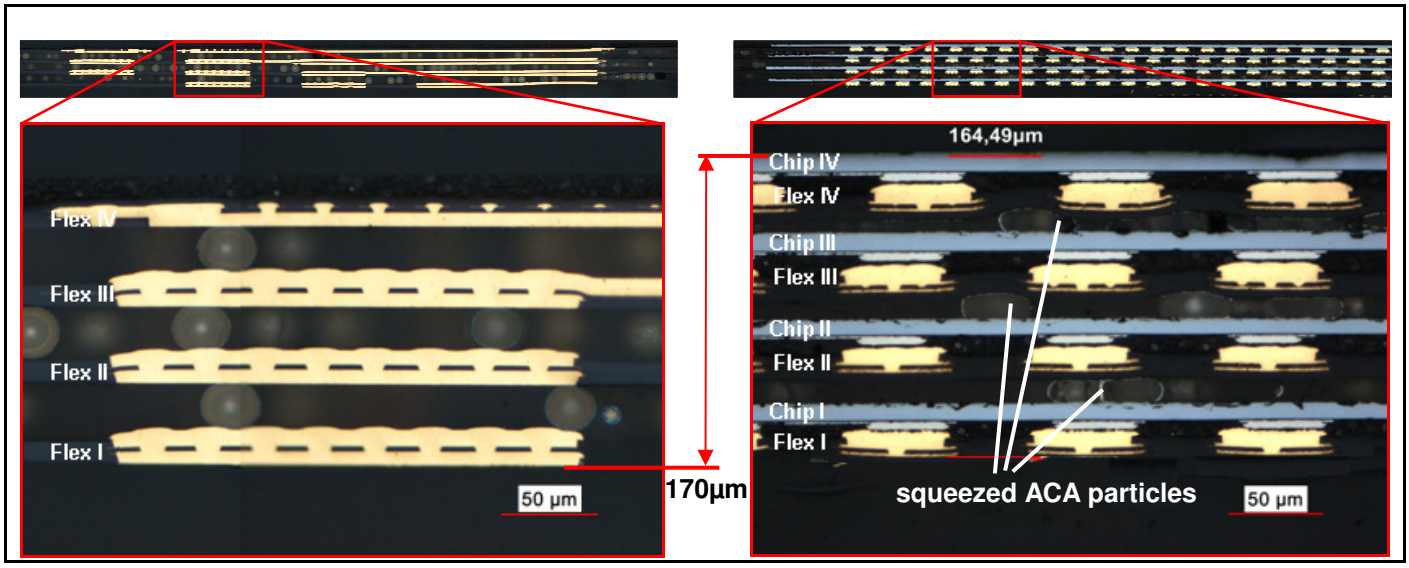
The set of non-functional test structures characterizing the interconnections between the 1st and 2nd interposer (Flex I-II) is simply traced back to the fact that essential pads have been covered with ACA from the previous flip chip assembly step, such that the interconnection to the next level interposer has failed. As this only affects the pads directly located close to the chip, this issue is limited to such single eight 4-Point-Kelvin patterns between the 1st and 2nd interposer only (figure 9). Therefore, the effect of different pad sizes on the contact resistivity between the interposer levels could not have been studied.



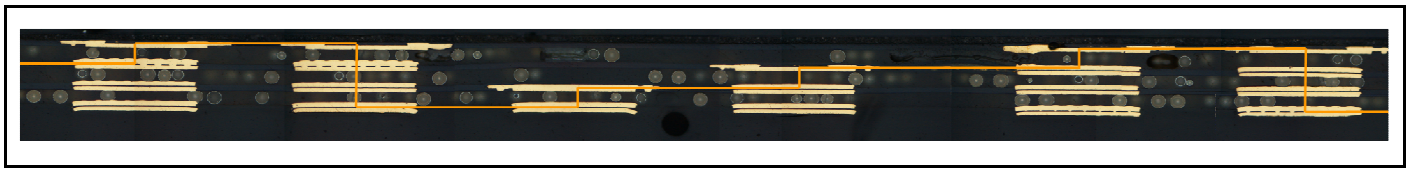
a) 4-Point-Pads b) covered with ACA

Figure 9: ACA spreading and pad covering on Interposer

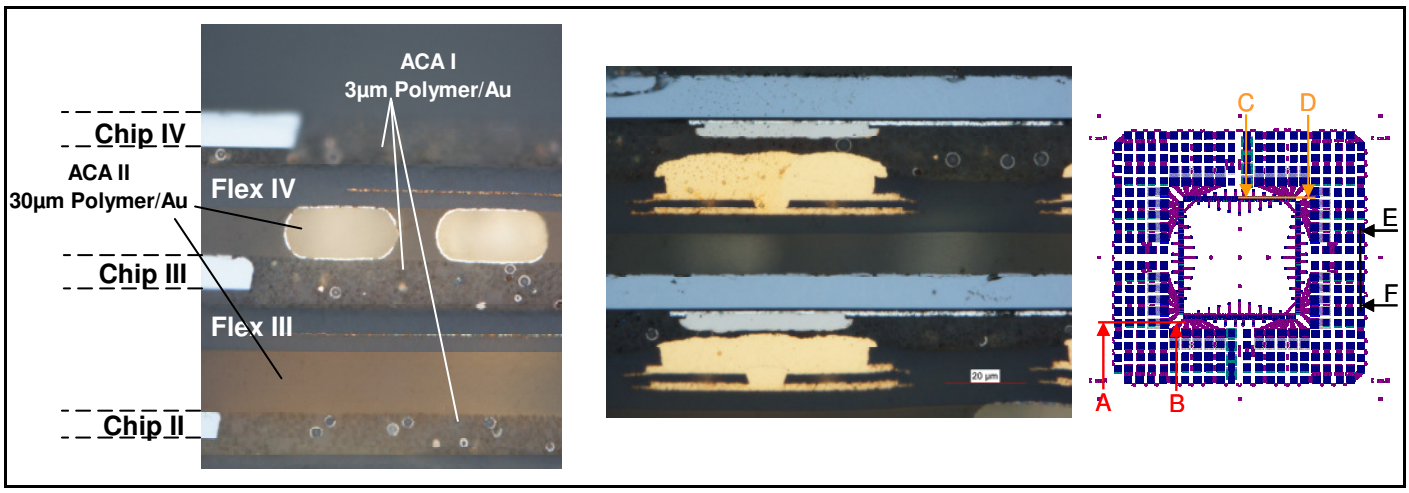
Selected cross-sections are depicted in figure 10.



a) ACA interposer interconnects, cross-section A-B b) ACA flip chip interconnects, cross-section C-D



c) Daisy-Chain interposer I–IV, signal path, cross-section E-F

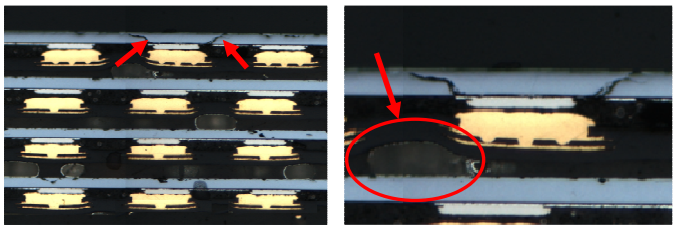


d) layers in detail close to the chip edges e) ACA flip chip interconnects f) cross-section positions

Figure 10: cross sections of the chip stack module

The locations of the cross-sections can be seen in figure 10f). The highly coplanar assembly has a final thickness of 170 µm (figure 10a), b)). Thickness tolerance from left to right (l=10 mm) is less than 5µm. The chips in the lower three levels (I, II, III), having typical ACA interconnections (details in figure 10e), are embedded between the ACA layers or interposers respectively (figure 10b). Nearly the same distances between the chips have been reached. The top ACA layer, making contact

between level III and IV, is compressed to a slightly higher extent than particles between level I-III, which has been considered the reason for the chip Daisy-Chain failures (compare figure 8, chip 4). Obviously, the accidentally applied (over-) load has caused chip cracking such that single, far in excess deformed, ACA particles has locally induced stress peaks (figure 11).



a) cracked Si b) crack inducing ACA particle

Figure 11: chip cracking

Apart from that, by using adapted bonding parameters (lower three levels) with hence less deformation of the ACA particles above the chips, the chips apparently stay in good conditions. ACA particles, interconnecting the interposers show moderate deformation and good contact (Figure 10a). Particles with a diameter of 30 µm easily bridge the necessary gap between the interposer levels. Figure 10c) reveals part of the stepwise circumferential Daisy-Chain structure with indication of the signal path. Details of the iterating layer sequence of Flex/ACAI/Chip/ACAII are shown in figure 10d).

4. Packaging Options

Waferlevel ACA

As aforementioned, application of the standard ACA process for the flip chip assembly is critical, especially the ACA application of common materials with common dispensing equipment having limited accuracy. Due to the fact that the entire area below the chip needs to be filled on the one hand and preferably ACA flow beyond the chip edges should be avoided on the other hand, the process tolerances are very tight. Here, application of ACA on waferlevel is considered the most promising technology, as, more or less, the optimal amount and distribution of adhesive can be reached.

First developments of waferlevel-ACA have shown promising results (figure 12).

a) chip left b) chip center c) chip right

Figure 12: waferlevel-ACA distribution after bonding, Si thickness 600µm

A thin bondline below the chip (5 µm particle diameter) together with a relatively small volume of ACA with an even shape along the chip edges could have been reached. Here, beyond further developments at Fraunhofer IZM, several other groups are working on the development of waferlevel-ACA, generally expected to have many advantages [19, 20, 21].

Chip/Interposer-area ratio

The present technology demonstrator module has a chip/interposer-area ratio of ¼. There is a large potential for miniaturization, considering that part of the area is taken by only interposer characterizing test structures at the expense of the final chip/interposer-area ratio. Additionally, a quite relaxed interposer interconnection pitch (lines/space: 250/200 µm) has been chosen. Here, further reduction in combination with even smaller ACA particles (<30 µm diameter) seems possible.

For each application, the final possible chip/interposer-area ratio needs to be separately identified, as it depends upon several parameters as e.g. chip size, number of I/Os (common, separate), chip interconnection pitch, chip thickness, number of levels and flip chip ACA distribution.

Interposers

As described above (2. Concept), for the majority of applications, the stacking technology is presumably limited to a reasonable maximum flip chip assembly thickness (<20-50µm) whereas the interposer thickness is basically unlimited. Hence, there is principally a wide range of possible types of interposers as long as the main requirements (e.g. double-sided metal layers with vias and targeted interconnection pitch) are fulfilled. Neverthelss, as shown, the chosen thin film interposer technology, by far, facilitates the lowest stack profiles due to the possibility of ultra thin substrate generation (<20µm). Here, exclusively noble Au metallizations, fairly good for adhesive technology, have been applied. Considering further connection of the module, e.g. by using a ball grid array applied on the bottom side of the base interposer, other plating materials as Ni or Cu can also be used.

The current test modules have been assembled by stacking single chips and single interposers using a flip chip bonder. In terms of process optimization and higher throughput, chip-on-(thinfilm-) wafer and (thinfilm-) wafer-on-(thinfilm-) wafer also seem possible whereas both approaches may benefit from ACA application on waferlevel.

5. Conclusions

Within a feasibility study, prototypes of an ultrathin IC stack with a total thickness of 170 µm including 4 flip chip levels, have been assembled. Special attraction is provided by the fact that the assembly is reduced to a simple alternating flip chip stacking sequence of chips and PI thin film interposers by using ACA technology only. This is made possible by the use of ultra low profile flip chip assemblies (10-20 µm), such that the vertical distance to the next level may be bridged by anisotropic conductive adhesive. Simple DC test structures (4-Point-Kelvin, Daisy-Chain) have shown the basic electrical functionality of this concept. Main current issues, such as handling and assembly of ultrathin ICs are expected to meet with upcoming technologies such as waferlevel ACA. To be based on that, the assembly of a higher number of modules is planned, giving the opportunity for further studies such as process issues, possible yield and reliability. Additionally, estimation of the electrical performance, especially the frequency behavior and current carrying capacities will show the possible range of applications.

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