EMBEDDED ACTIVE DEVICE PACKAGING TECHNOLOGY FOR REAL DDR2 MEMORY CHIPS

Yin-Po Hung, Tao-Chih Chang, Ching-Kuan Lee, Yuan-Chang Lee, Jing-Yao Chang,
Chao-Kai Hsu, Shu-Man Li, Jui-Hsiung Huang, Fang-Jun Leu,
Yu-Wei Huang, Ren-Shin Cheng and Tai-Hong Chen
Electronics and Optoelectronics Research Laboratories (EOL)
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan
yinpohank@itri.org.tw

ABSTRACT
As high-speed, high-density, and high-performance are the primary IC development targets, packaging becomes a key technology to bring out the best performance of the ICs. In this paper an embedded chip packaged module is developed for high speed memory devices. Embedding of semiconductor chips into organic substrates miniaturized the size of the package. Moreover, stacking multiple layers of embedded components can allow an even higher capacity of devices and packaging density. In addition to wire bonding or w-BGA technologies, embedded package structure provides an alternative means to form redistribution circuits and electrical bonding pads. Meanwhile the electrical performance can be enhanced due to the wafer level package-like structure. Superior electrical performance is provided by forming shorter electrical path from chip pad to outer. In this study, a chip-in-substrate package (CiSP) using thin chips (~ 50um) of DDR2 memory with real function is disclosed by means of build-up technologies such as dielectric layer lamination, micro via drilling, and redistribution layer forming to implement the JEDEC-compliant DDR2 component. The PCB compatible process is a low-cost, high-yield, and versatile technology. Electrical performance similar to wafer level package and even better than wire bonding or w-BGA package can be achieved by adopting this proposed solution. A test vehicle of DDR2 memory with real function is studied to demonstrate the feasibility and electrical performance of this developed packaging. Relative process features will be presented to give a thorough construction of the package structure.

Key words: DRAM, embed, active device, package

INTRODUCTION
With the demand for electronic products towards high functionality, high-speed signal transmission and high-density of components, more and more products gradually come out in various types of BGA. Furthermore, the number of passive components has drastically increased, particularly in consumer electronics products such as VCRs, camcorders, cellular phones, etc. Therefore, how to accommodate a large number of electronic components in a limited space has become the developing task in electronic packaging industry. To solve this problem, packaging technology is gradually heading towards System in Package (SiP), in which 3D-IC package and integration of embedded components has become the key technologies. As the development of active components using chip scale package (CSP), flip chip technology or even 3D stacking technology to further reduce the volume occupied by all components in a single package, ITRI has started to develop the feasibility of combining active components with organic substrates. It is so-call the Chip in Substrate Package (CiSP) that provides the concept of the integration of active and passive components with relative substrate or PCB processes. It can also be regarded as a process integration of PCB substrate and silicon substrate that raised the package density and miniaturized the package volume. Meanwhile, the electrical performance is subsequently elevated due to the shortened conducting path. Embedding of active or passive components in substrate or built-up dielectric layers is the key technology for fabricating SiP. It allows heterogeneous integration that contains interconnection of deferent devices in a single package. Even 3D die stacking or package stacking can be achieved without the fabrication of through silicon vias (TSVs) [1]. Integration of multiple active and passive components with different sizes and circuit layout by means of built-up dielectric design, which is similar to traditional low cost PCB process, is thus the primary advantage of embedding technology applied in SiP.

On the other hand, the most problematic issue in the recent LSI package development is the reliability of the high-density flip chip ball grid array package in the use of low-k material [2]. Interfacial delamination and cracks in the material during package assembly may result from a coefficient of thermal expansion mismatch between the LSI chip and substrate. From a technical point of view, embedded IC technology is an advanced process which omits the traditional micro-interconnection process in solder bumping and underfill dispensing. Package can be fabricated with built-up dielectric and direct Cu interconnection without solder joints, thus high stress concentration can be avoided if low stress dielectric

material is adopted in the package [3]. Although there are unique advantages of using embedding technology, the primary difficulty lies in how to handle the links of metal pads and traces in chips and substrates by the concept of PCB manufacturing processes. However, there are several challenges in using liquid dielectric materials for chip burying, especially via forming on the FR4 substrate in which warpage has occurred. Uniformity and co-planarity are obviously limited that would affect the lithography and follow-up processes. In order to acquire a flat and nearly bulge-free dielectric layer, it is necessary to adopt a low stress and highly compact dielectric material and built-up process. For the aforementioned reason, the use of vacuum lamination of film type dielectrics for embedding chip in substrate and via forming using laser drill process are the key developing technologies in embedded chip packages. Due to the B-stage characteristic of the low stress film type dielectric material, the built-up dielectric layer can be fabricated as a void-free, compact, and nearly bulge-free surface.

EOL/ITRI has developed the technology of CiSP for many years. It was started from a single chip embedded in organic substrates to multi-layer of re-distribution circuits built-up over the semiconductor component in different aspects of application and functionality [4-5]. Novel development such as chip in film or embedding thin film capacitor using high dielectric constant material as passive component have been studied in the past few years. In recent research, semiconductor chips with real functions are gradually applied into the CiSP to investigate the functional performance of the package. In this study, a chip-in-substrate package (CiSP) with thin chips (~ 50um) of DDR2 memory with real function is disclosed using built-up technologies such as dielectric layer lamination, micro via drilling, and redistribution layer forming to implement the JEDEC-compliant DDR2 component.

PACKAGE STRUCTURE DESIGN

Figure 1 shows the outline and layout of a DDR2 real die provided by ChipSip Technologies Inc., where a package size of 10.5 mm x 13.0 mm x 1.2 mm with 60 I/O balls at 0.8 mm-pitch is required. W-BGA is the current package for this device and wire bonding is adopted to electrically connect the central pads to a flexible BGA substrate which is attached to the chip, as shown in Fig. 2 [6]. In this study, embedded chip into organic substrate with built-up dielectric and redistribution layer is applied to replace w-BGA and wire bonding technology. The CiSP structure for this DDR2 test vehicle is designed as shown in Fig.3. The electrical connection is formed by micro-via forming and metallization rather than wire bonding. Meanwhile, the redistribution layer on the dielectric can be formed together with micro-via filling rather than a pre-formed and patterned substrate. It has been proved to provide a good reliability performance in previous study with daisy chain structural test vehicle [4]. Thus, to examine the feasibility of CiSP for high speed memory chips, DDR2 chips with real function are introduced into the embedded structure.

By proper combination of the materials such as FR4 substrate, dielectric and die attach film used in this structure, and together with the relevant well-controlled processes, the CiSP structure with embedded real DDR2 chip can be accomplished. The detail description for each core technique has been disclosed in former study [4]. In the next section, only some characteristic methods and encountered tasks will be disclosed.

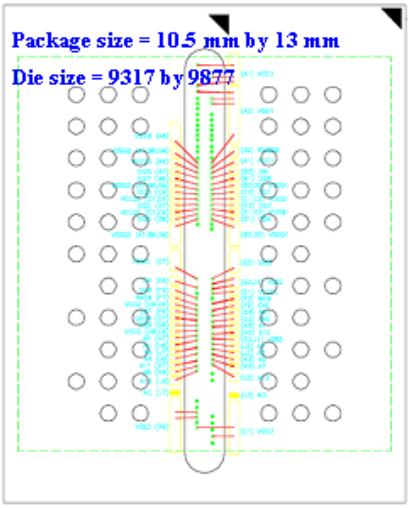

Figure 1. The package outline of the DDR2 provided by ChipSip Technologies Inc.

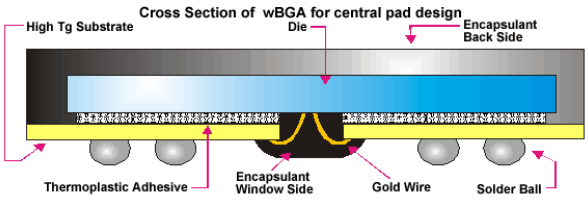

Figure 2. Conventional w-BGA structure [6]

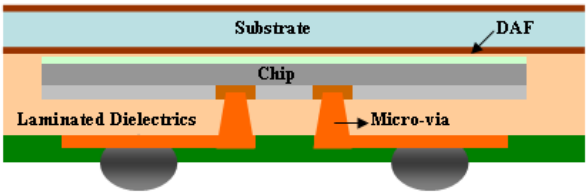

Figure 3. CiSP structure for memory chips

PROCESS METHODS

The schematic process flow for applying DDR2 chip in CiSP is shown in Fig. 4. It begins with a 600 um-thick FR4 substrate provided by Hitachi Chemical (MCL-E-679FG(S)), which is a halogen-free, high elastic modulus and low CTE multilayer material. Surface treatment of brown oxidation process is used on the Cu surface of the substrate to provide a roughened surface to obtain a better adhesion for die attach film and dielectric layer. The DDR2 chip which is thinned to 50 um-thick is vacuum laminated with 10 um-thick die attach film provided by Nitto Denko (EM-700) in the back plane. Die bonding is proceeded with SÜSS Microtec FC-150 to reach high bonding accuracy. After die bonding, die embedding is performed by the lamination of an 80 um thick ABF (Ajinomoto built-up film, GX-13R) by means of vacuum lamination with the aid of MEIKI 2-stage Vacuum

Laminator and then thermal cured. Once the die is embedded in ABF, via holes are formed by laser drilling with Siemens Dematic Microbeam 3200 with a 355 nm wavelength. Subsequent via and RDL patterning are performed with a series processes including electroless Cu plating as seed layer, photolithography, Cu electroplating, photoresist stripping and micro-etching of seed layer. Finally, solder mask printing and ball mounting are provided to complete a single CiSP, as shown in Fig. 4. For the further package stacking applications, conductive vias can be formed through the dielectric layer and substrate as a package-on-package form. Principal specifications of the CiSP structure are listed in Table 1.

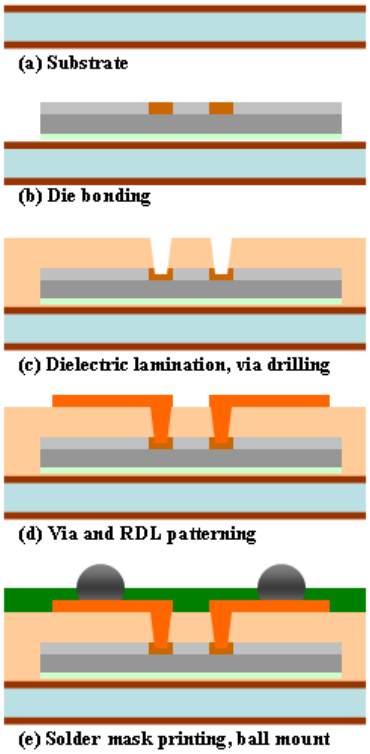

Figure 4. Schematic process flow of CiSP

Table 1 Principal specifications

Die	9.3x9.8 mm-size, 50 um-thick
Die pad	70 x 70 um-opening, 90 x 90 um-pad
Substrate	600 um-thick high Tg FR4
Adhesive	Die attach film (DAF) 10 um-thick
Dielectric	ABF 40 um-thick x 2
Via	50 um-diameter

The detailed description for each core technique including die bonding, lamination, laser via drilling and structuring, via metallization and patterning, has been disclosed in former study [4]. In this paper only some characteristic and encountered tasks will be addressed here.

Lamination, De-Smear, and Micro-Etching

The dielectric material used in this research is ABF (Ajinomoto built-up film, GX-13R), which is compatible with the semi-additive process (SAP) technology and could perform fine line/space with better reliability. It has been disclosed in the literature [7] that the considered appropriate dielectric thickness above chip pad is 15~20 um. It is found in this research that when the ABF above the chip pad is too thin (about < 10 um), the dielectric layer is easily to be over-etched during the de-smear process, especially those on the corners of the chip, as shown in Fig.5.

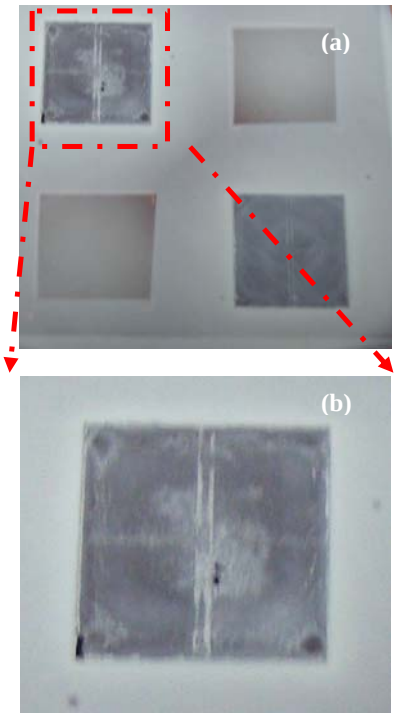

Figure 5. (a) Over-de-smeared dielectric surface, **(b)** enlarged view

De-smear is a means of micro-etching used to clean the drilled vias and increase the roughness of ABF surface for the adhesion with Cu. The electroless Cu plating is sequentially processed to deposit a Cu seed-layer of about 1 um thickness on ABF surface as the bottom electrode of electroplating. Photolithography is then applied to define the electroplating patterns on the dielectric layer. A layer of 12 um thick Cu is electroplated here and then the photoresist is stripped. Finally, the Cu seed layer is etched away to form the redistributed layer. While processing Cu etching, it is found that there is still some Cu residue on the dielectric layer, as shown in Fig. 6, which may cause circuit shorting. Though a longer period of etching is proceeded to clean the residue, some of the patterned RDL would be damaged at the same time.

The Cu seed layer etching process uses nitric acid to eliminate the remained Cu. Copper would not be inactivated in nitric acid solution and with the increasing consistency of nitric acid, the etching rate would also be elevated. The reaction between Cu and nitric acid can be represented as the formula listed below:

$$2Cu + 6HNO_3 \rightarrow 2Cu(NO_3)_2 + 3H_2O + 2NO \uparrow + NO_2 \uparrow$$

As a result of de-smear process, the roughened ABF surface is an enhancement for electroless Cu to compactly deposit on. However, if de-smear process prolonged to cause strong anchoring of ABF and electroless Cu, it would be difficult to completely remove the Cu seed layer, as shown in Fig. 6. According to the situation we have encountered, a series of experiments were take into consideration including the consistency of nitric acid used in the etching process and the de-smear period. By well adjusting the parameters, the patterned circuits can be well defined without any Cu residue, as shown in Fig.7. Full and half time of standard de-smear process in the etching stage are consulted. Meanwhile, nitric acid of 25 % (standard) and 40 % in consistency are taken into account for the experiment. It is found that the de-smear process determines the effect of the elimination of Cu residue. The Cu seed layer in the sample using half time de-smear process and standard 25 % nitric acid can be totally removed.

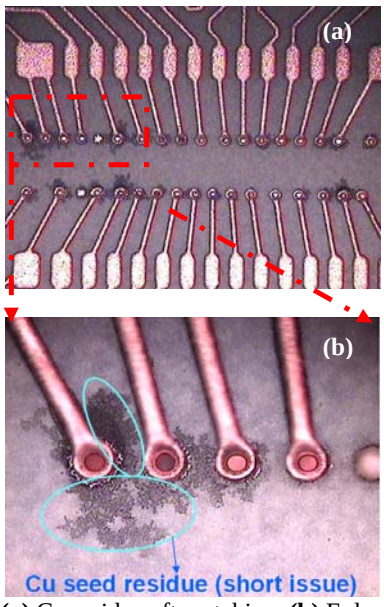

Figure 6. (a) Cu residue after etching, **(b)** Enlarged view

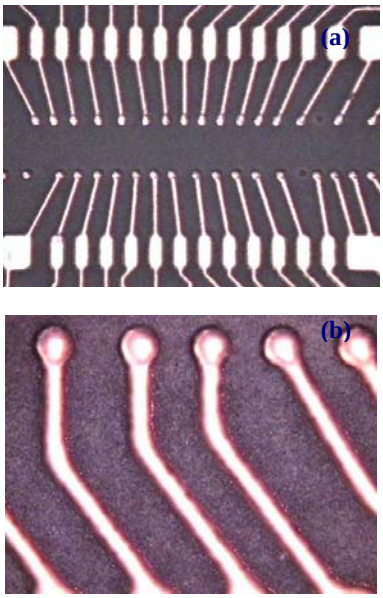

Figure 7. Cu residue completely removed

RDL Patterning Methods

At first, the patterned re-distribution layer (RDL) was fabricated using Sn mask for Cu wet etching to lower the fabrication cost. The process began with electro-plating Cu on the dielectric layer. Subsequently a thin layer electro-plated Sn was deposited on the electro-plated Cu as an etching mask. Laser hatching on the electro-plated Sn was proceeded to expose the etching parts of electro-plated Cu. After etching the electro-plated Cu, the electro-plated Sn was subsequently removed and the etched electro-plated Cu pattern was revealed.

Although the cost of masks can be saved using Sn mask as an etching medium, electro-plated Cu pattern would be easily undercut during the etching process, as shown in Fig. 8. Therefore, in the follow-up processes, the use of the mask still can not be spared. The process thus becomes using photolithography including dry film laminated on the electroless-plated Cu seed layer and photo developing the photoresist to define the electro-plating pattern. Subsequently, the electro-plating Cu is conducted and the photoresist is removed. Finally the seed layer Cu is also etched to reveal the expected RDL pattern, as shown in Fig. 9.

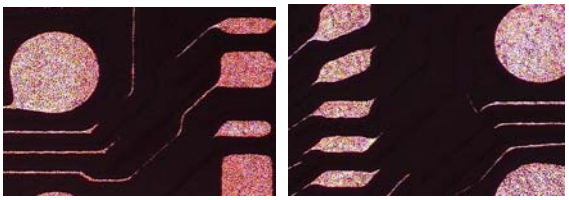

Figure 8. Undercut after Cu etching and Sn mask removing

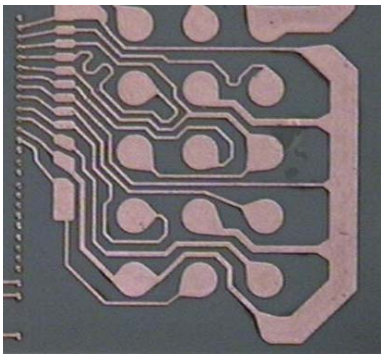

Figure 9. RDL pattern using photolithography

FUNCTION TEST

After the RDL patterning, standard solder mask printing, ball mount and singularizing were provided to complete a single DDR2 embedded package. Figure 10 shows the accomplished DDR2 chip embedded package, which is singularized as 13 mm x 10.5 mm in size to implement the JEDEC-compliant DDR2 component. The thickness of a single package is measured as 1.2 mm, which also fits the JEDEC requirement.

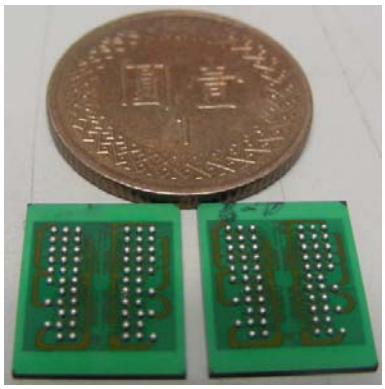

Figure 10. DDR2 chip embedded package

Function test was evaluated by means of direct soldering a single package on conventional DDR2 DIMM module, as shown in Fig. 11. The DIMM module was directly mounted on the memory socket of a conventional PC main board to execute the function test. The operation frequency was set as 266, 333, and 400 MHz, respectively. The DIMM module can still maintain its workability under these test frequencies.

Figure 11. Function test of DIMM module including DDR2 embedded package

RELIABILITY

To investigate the reliability of the embedded package, some specific measuring pads were selected form the BGA to check the open/short of circuits. It is because the module is not a daisy-chained dummy package but a workable real die embedded package. On the other hand, a real-time function tester is currently not available in this research group. Therefore, for the sake of simple and convenience, the open/short of the specific circuit pads was presently regarded as the criterion for pass/fail evaluation.

Pre-condition test was adopted as the first examination before the posterior tests. Samples which did not pass the pre-condition test would be excluded for the next tests such as thermal humid storage test (THST) or thermal cycle test (TCT). In the pre-condition test, samples were firstly baked 24 hours at 125^{o}C, and then stored in 30^{o}C/60%RH for another 192 hours. Reflow for three times at a peak temperature of 260^{o}C was subsequently performed after the 192 hours 30^{o}C/60%RH storage.

In the pre-condition test, 18 samples were put into examination and no failure occurred by means of open/short detection. It is also seen that there is no de-lamination, void, deformation or other defect observed at the interfaces after pre-condition test. In fact, before this successful pre-condition test, this embedded package had been experienced de-lamination. But after a series of process modification, the most optimum package had been carried out and those aforementioned defects were prevented. The subsequent reliability tests are still in progress and the results will be orally reported at the conference.

CONCLUSIONS

In this paper, the embedded DDR2 chip with real function was successfully developed. The structure incorporates the advantages of WLP and embedding technology and implements a workable DDR2 module component. It is expected that the electric performance would be better than the conventional w-BGA package. Function and performance tests including component level and board level are now on-going. Moreover, a benchmark study with w-BGA will be setup to verify the applicability to mass production. Similar approaches will not only applicable to memory module but also other high-speed applications such as CPU, graphic, or chip set. EOL/ITRI now is developing the embedding technology on communication modules, which includes not only active devices but also embedding passive capacitors. It is believed that such an embedded structure will still provide the advantages of short circuit length and high package density.

ACKNOWLEDGMENTS

The authors would like to appreciate the support from the Department of Industrial Technology, MoEA Taiwan, R.O.C. Also the technical supports from Ray Wu, Ato. Tech., DRAM wafer and function test from ChipSip Tech., FR4 substrate from Hitachi Chemical, Die attach film (DAF) from Nitto Denko, ABF from Ajinomoto Fine-Techno, flux and solder ball from Senju metal industry.

REFERENCES

1. T. Funaya et al., “Ultra thin die embedding technology with 20um-pitch interconnection“, Proc. 60th Electronic Components and Technology Conf., Las Vegas, NV, June 2010.
2. L. L. Mercado et al., “Analysis of flip-chip packaging challenges on copper/low-k interconnects”, IEEE Transactions on Device and Material Reliability, Vol. 3, No. 4, December 2003, pp. 111-118.
3. K. Mori et al., “Reliability of thin seamless package with embedded high-pin-count LSI chip”, Proc. 60th Electronic Components and Technology Conf., Las Vegas, NV, June 2010.
4. C. T. Ko et al., “Embedded active device packaging technology for next-generation chip-in substrate package, CiSP”, Proc. 56th Electronic Components and Technology Conf., San Diego, CA, May 2006.
5. L. C. Shen et al., “Thermal and electrical performance enhancement with a cost-effective packaging for high speed memory chips“, Proc. 57th

Electronic Components and Technology Conf., Reno, NV, May 2007.
6. http://www.utc.com.tw, US PAT. 6,190,943.
7. D. Manesis et al., “Innovative approach for realization of embedded chip packages – technology challenges and achievements”, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, May 2009.