

**IMAPS International Conference on Device Packaging**  
**March 9-12, 2009**



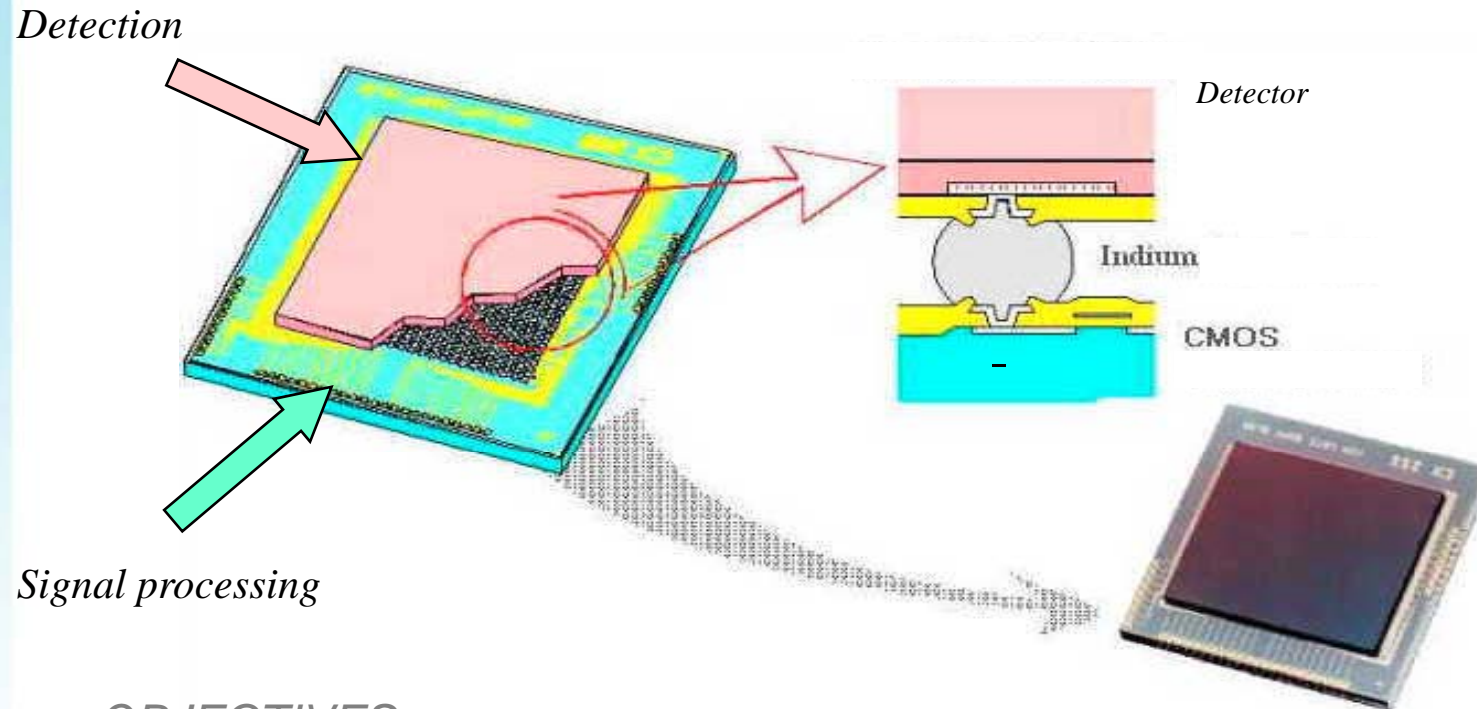
**Electrical characterization of high count, 10 $\mu$ m pitch  
room temperature vertical interconnections**

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# Introduction

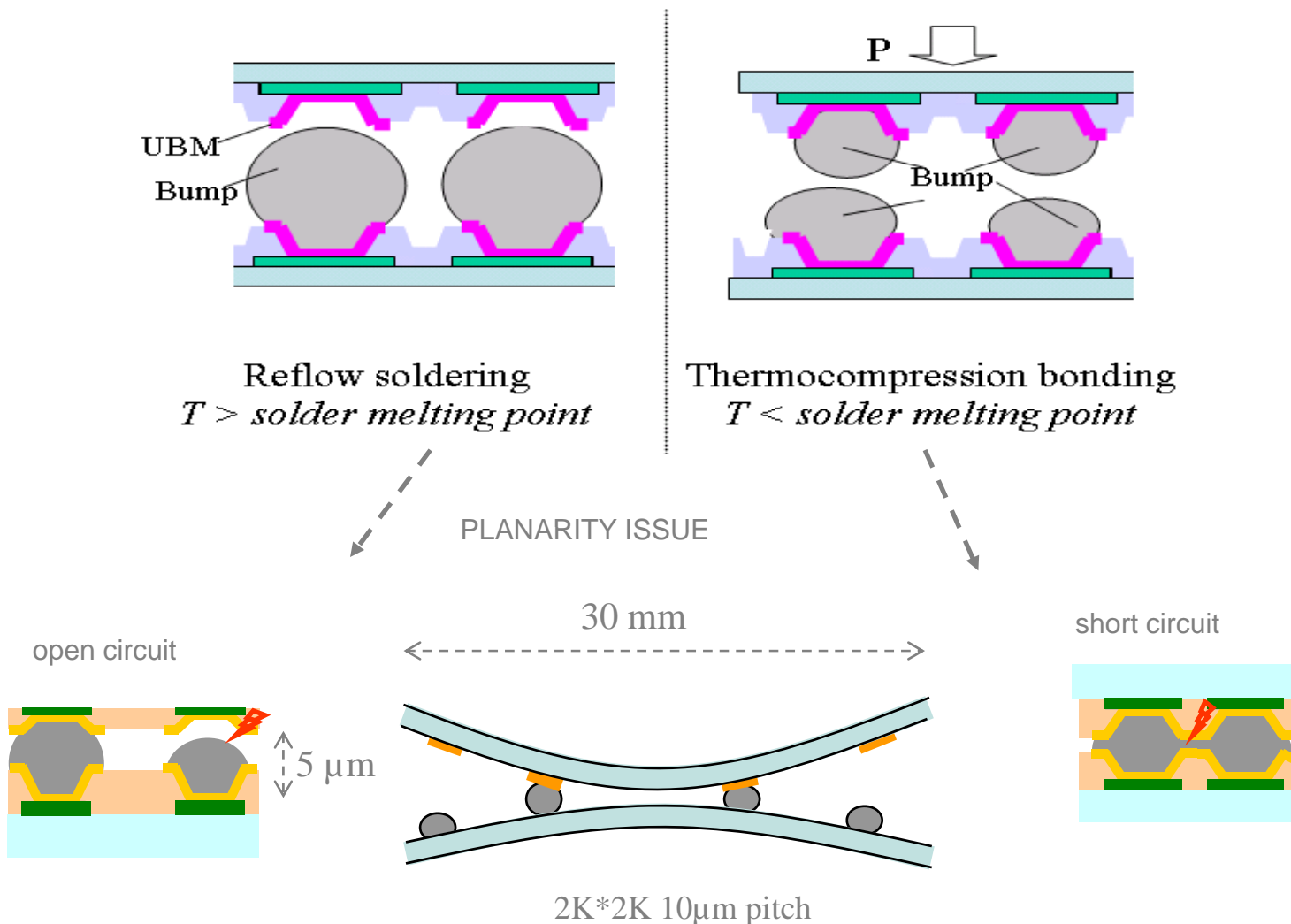
## Heterogeneous imaging arrays



### OBJECTIVES

- Increase pixels count (up to 4 million)
- Reduce connection pitch (down to  $10\ \mu\text{m}$ ,  $5\ \mu\text{m}$ )

# Flip-chip soldering techniques/ issues



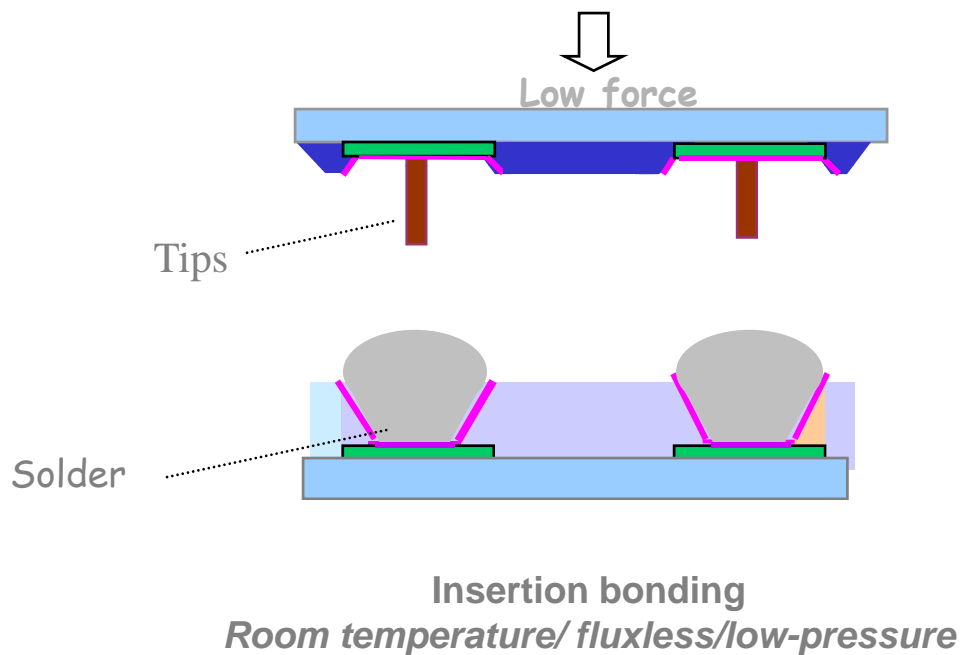
# Other solutions ? ?

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- Overcome planarity issues :
  - Lower chips planarity requirements
  - Lower bumps height uniformity requirements
- Simplify flip-chip process
  - Room temperature
  - Fluxless
  - Low force
  - No clean

# New approach

Insert hard tips in solder lands

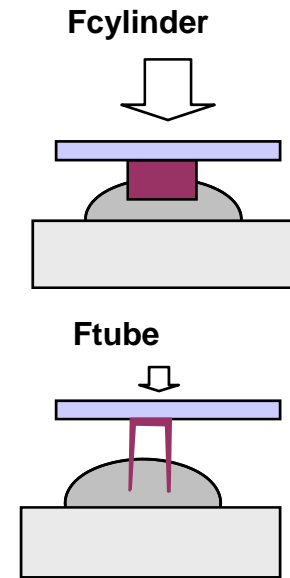
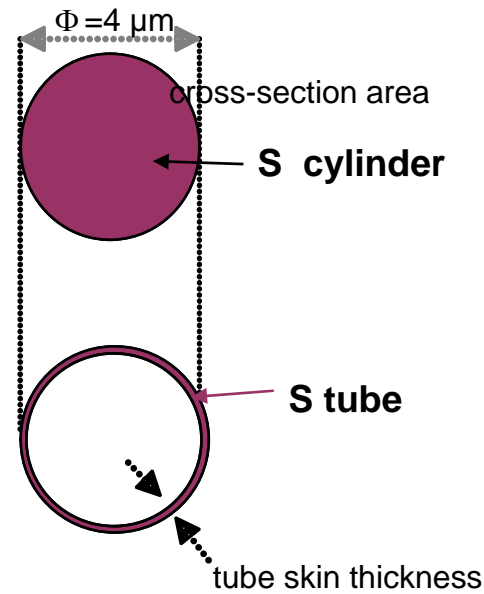
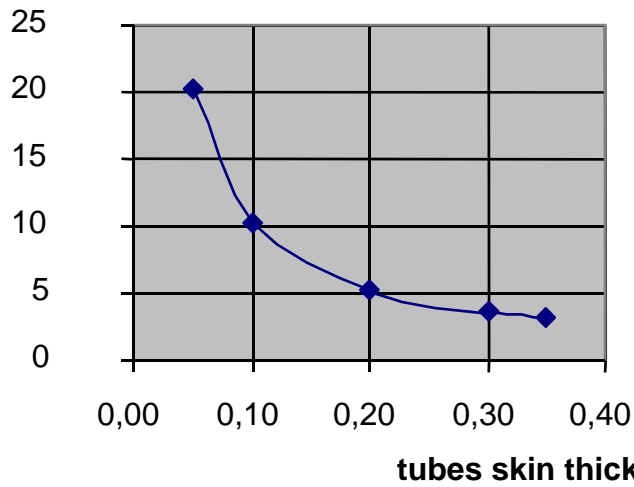


# Micro-tubes as tips?

First approximation: postulate insertion force proportional to micro-tip cross-section :  $F_{tube} = F_{cylinder} * (S_{cylinder} / S_{tube})$

Expected insertion force reduction

$S_{cylinder} / S_{tube}$



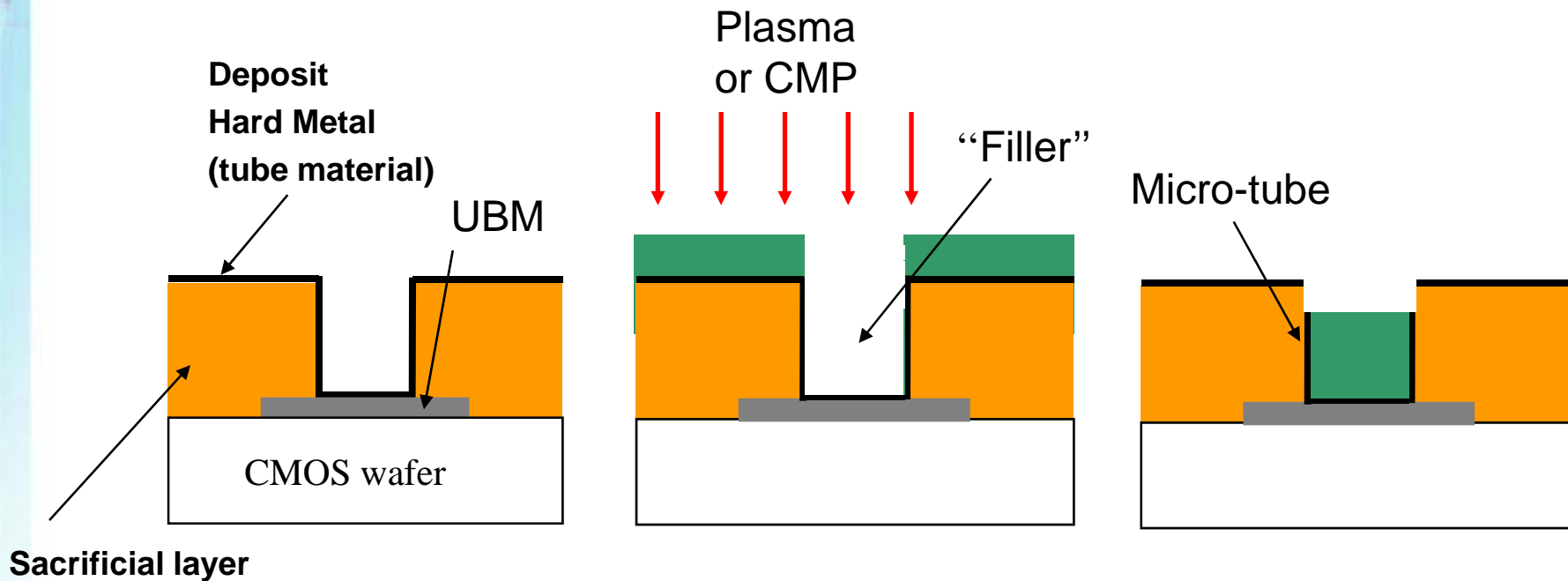
# Micro-tubes fabrication

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Define process sketch to build  
4 million micro-tubes at 10  $\mu\text{m}$  pitch ?

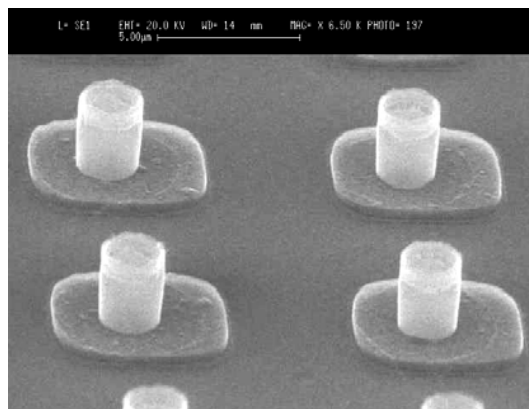
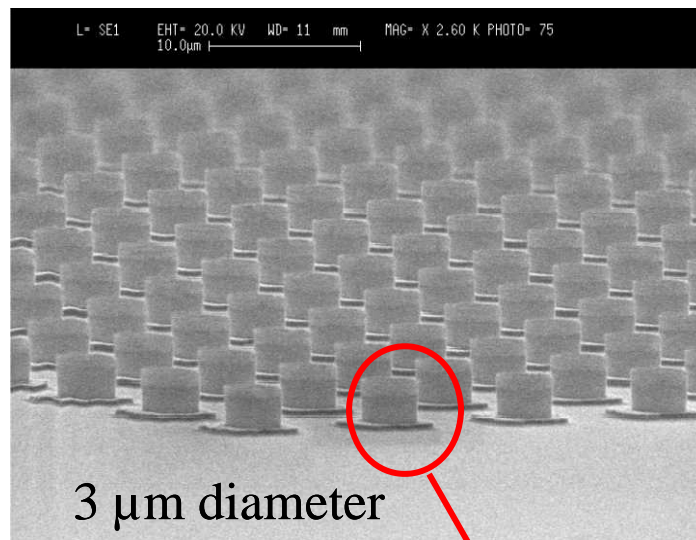
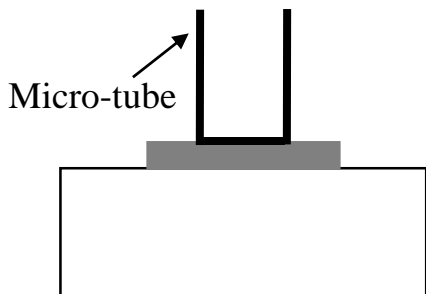
# Micro-tubes fabrication sketch

« Gap fill » process sketch:

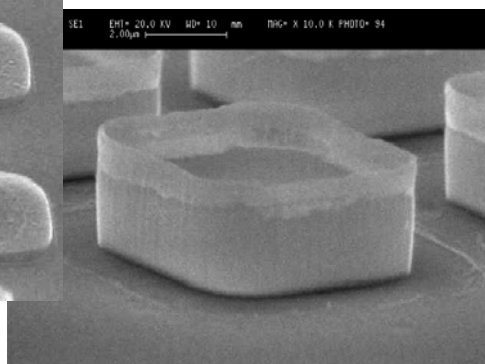


# Micro-tube fabrication (10 $\mu$ m pitch)

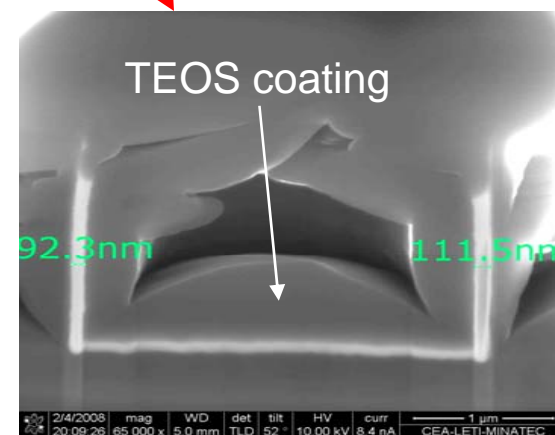
## Process flow (2/2)



2  $\mu$ m diameter



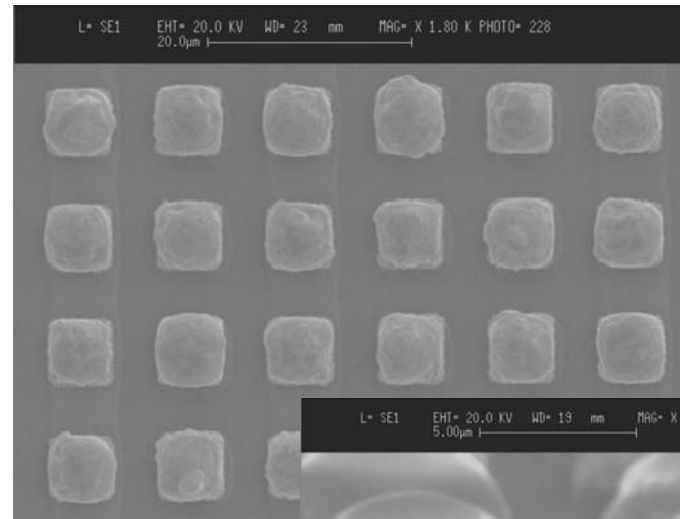
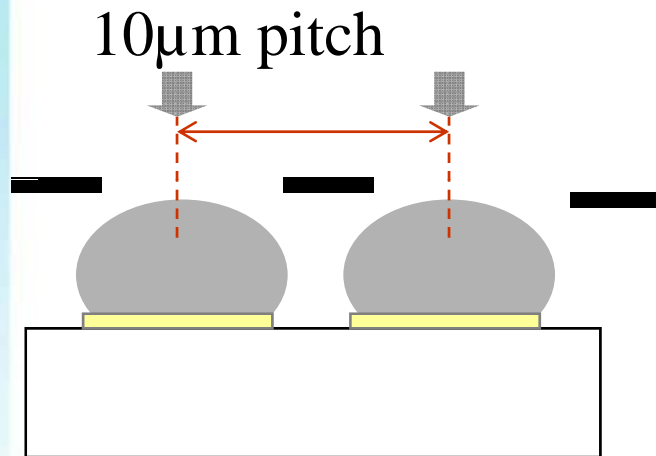
8  $\mu$ m diameter



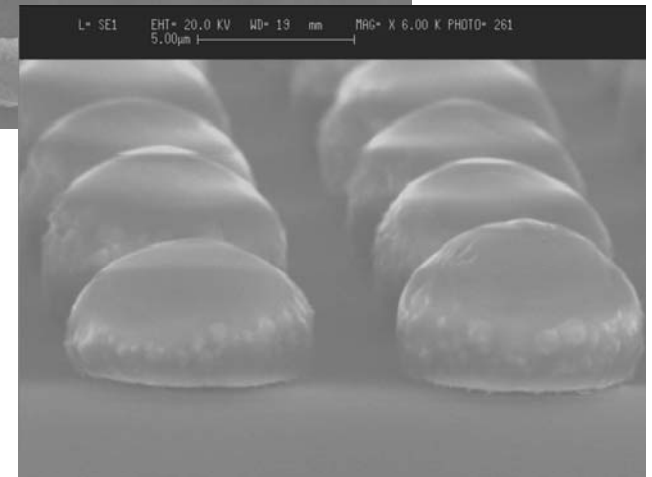
Cross section of 3 $\mu$ m diameter tube

# Micro-bumps fabrication (10 $\mu\text{m}$ pitch)

## Microbump (liftoff process)



Before reflow



After reflow

# Insertion Results

## Flip-chip bonder

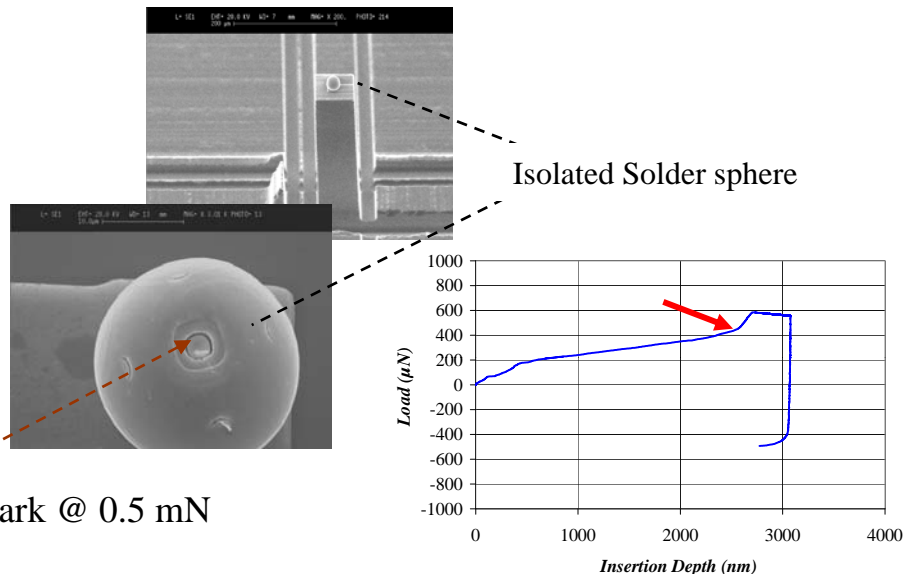
- Assembly: SET<sup>®</sup> FC300
  - 300mm capability
  - Post bond accuracy:  $\pm 0.5 \mu\text{m}$  (3 sigma)
  - Force range up to 4 000 N
  - Chuck / head : 20°C to 450°C



# Insertion Results

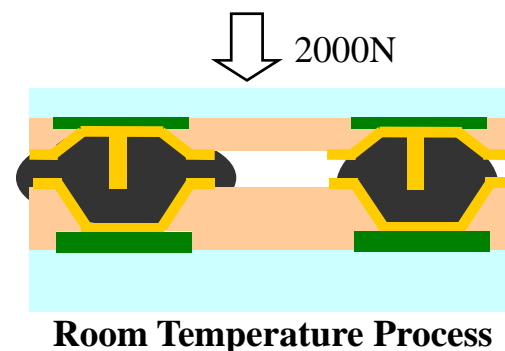
Determine insertion force/dwell time...

- Single tube insertion  
Measured load: 0.5 mN / tube  
(using nanoindentation technique)



Single tube insertion mark @ 0.5 mN

- Array insertion  
Calculated load for 4 millions simultaneous connections = 2000N

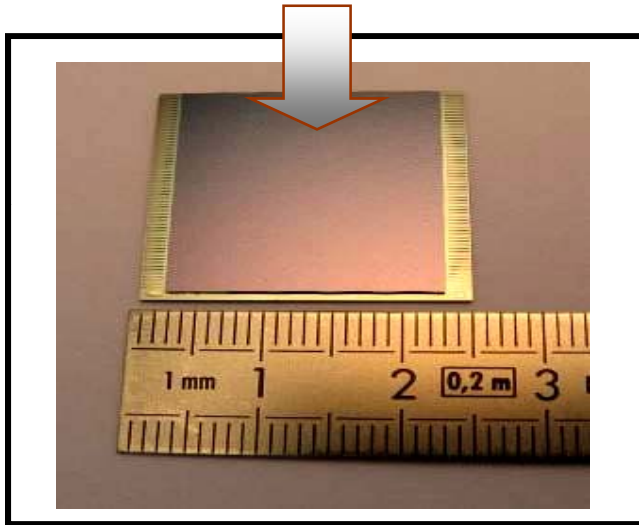


# Insertion Results

Insertion process (making)

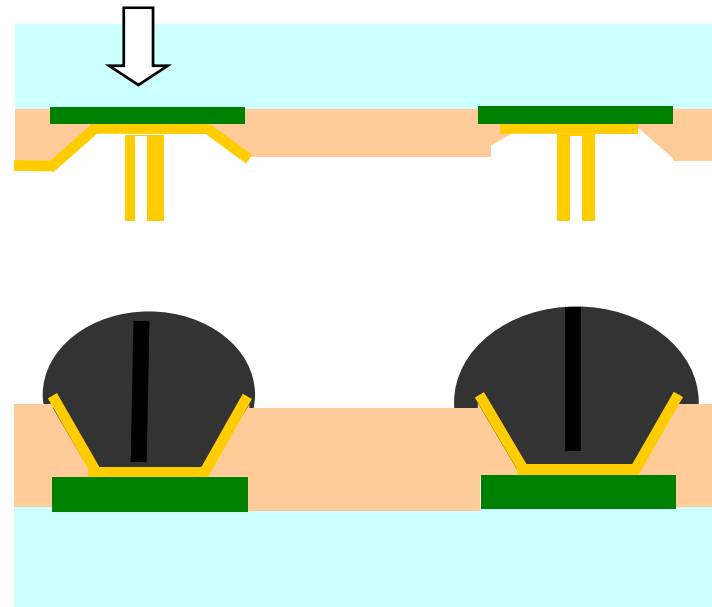
**2000 N**

*4 megapixels array*

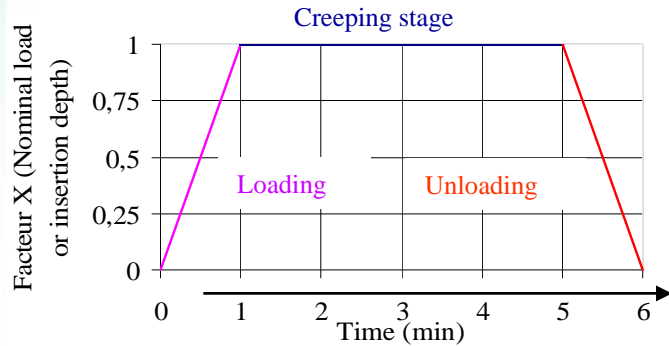


**0.5 mN**

*Single tube*



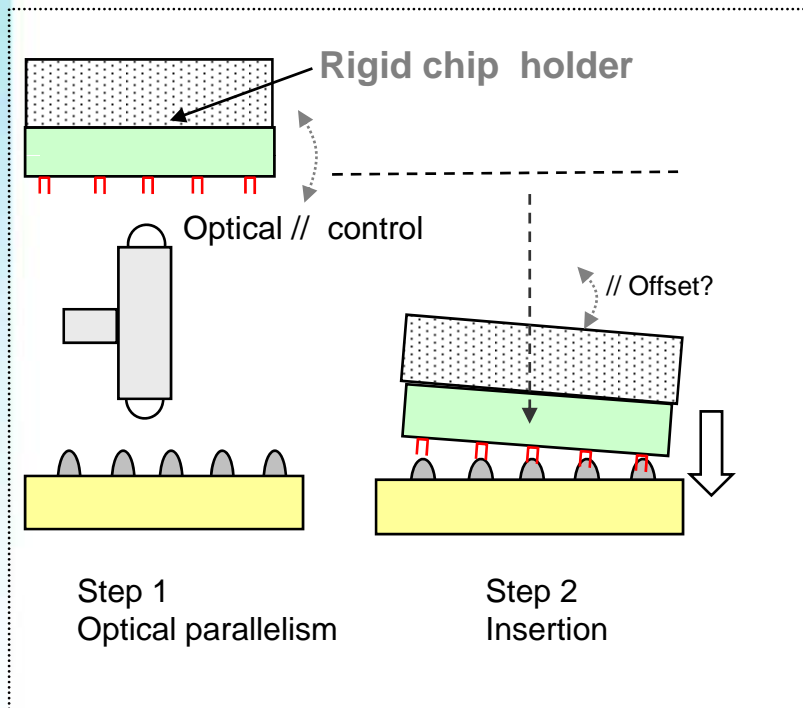
**Room Temperature Process**



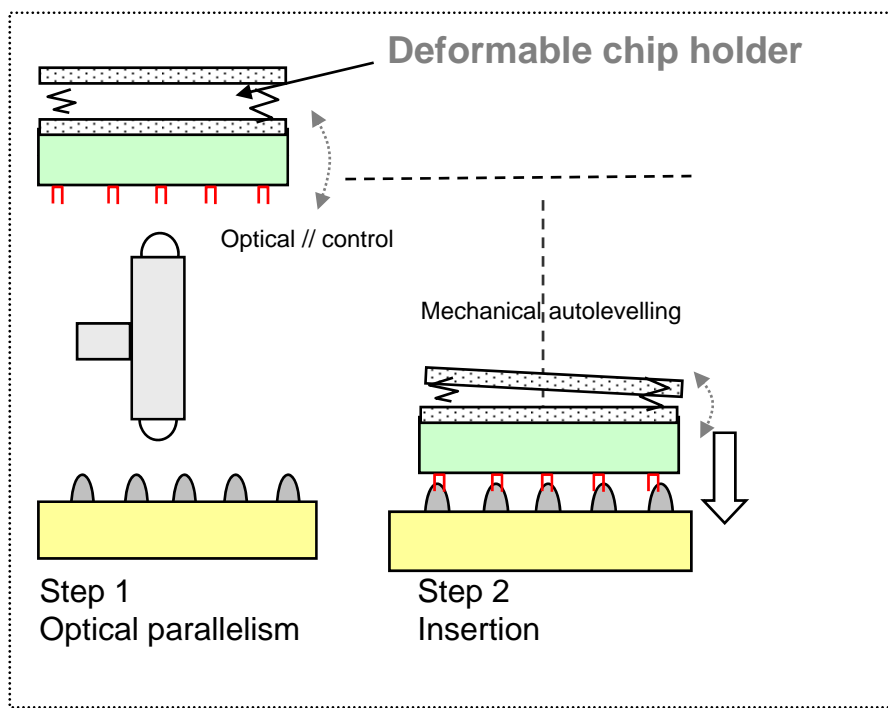
# Insertion Results

## Parallelism control experiment

### Experiment 1: standard parallelism



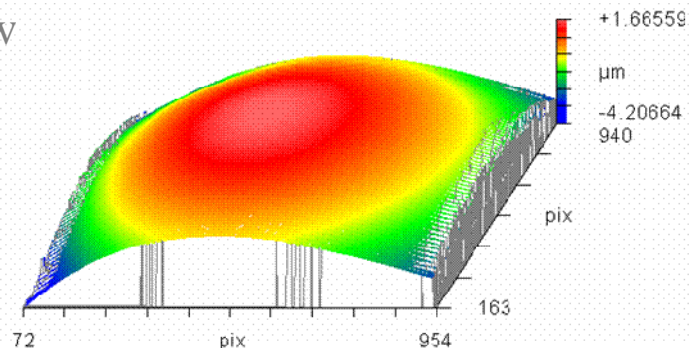
### Experiment 2: parallelism + autolevelling



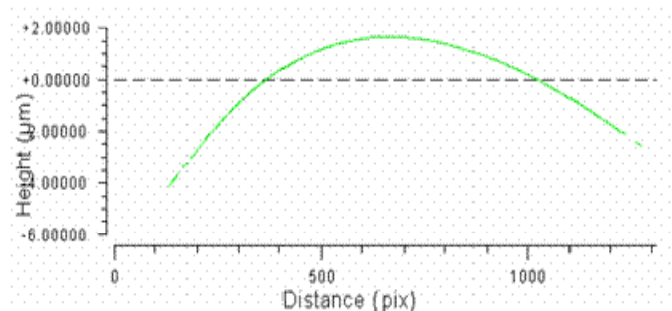
# Insertion Results

## Chips planarity before insertion

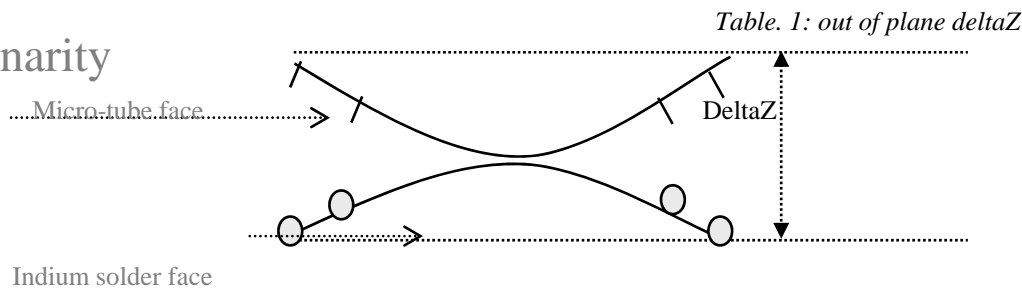
3D View



2D View



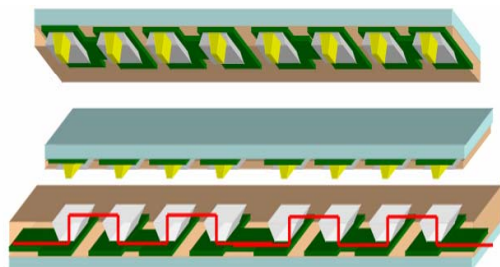
## Overall Planarity



Experiment 1	Experiment 2
8.3μm	8.1μm

# Electrical results

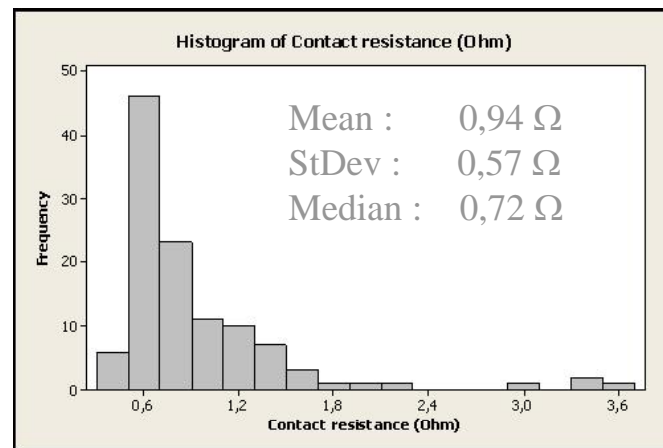
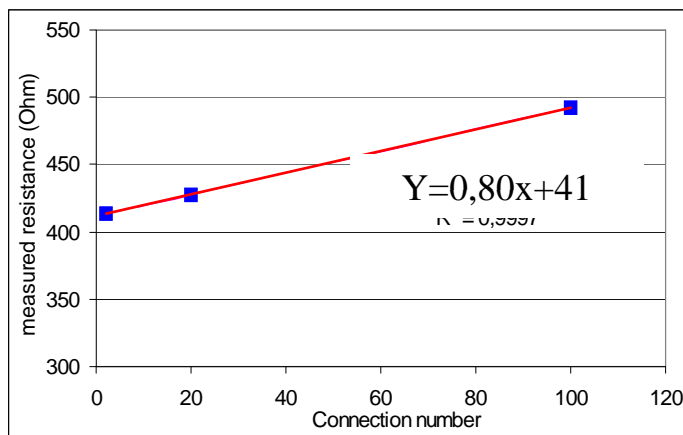
## Multi Daisy chains test vehicle



Extraction of:

- Mean contact resistance per connection
- Open circuits/ yield mapping
- Short circuits/ yield mapping

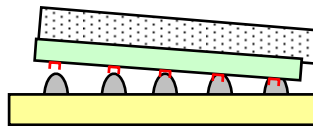
## Contact resistance per connection : results



# Electrical results

## Connection yield : open and shorts

**Experiment 1=**  
without autolevelling



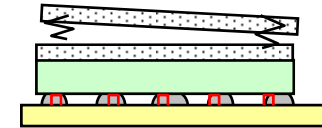
Without autolevelling

98,6	99,1	99,1	98	99,1	99,1
99,6	98,6	99,1	97,3	98,6	99,1
99,6	100	100	97,3	100	100
98	100	100	99,1	99,6	100
99,6	99,6	100	98,6	100	99,6
94,7	93,3	100	98	98,6	99,6
98,6	99,1	95,7	99,6	97,3	100
88,3			88,3	93,3	95,7

**75.3% connected**  
**0% shorts**

Connection (%)  100%  [100-98] %  
 Mean array connection yield 75,3 %  
 Mean array Short circuit defects (<0,01%)

**Experiment 2=**  
With autolevelling



With autolevelling

	93,3	98	98	95,7	93,3
	94,6	94,6	94,7	99,1	99,6
91,4	97,3	98	99,1	99,1	100
91,4	91,4	96,6	99,6	99,6	100
98	99,1	99,6	99,6	100	100
98	100	100	100	100	100
94,6	99,1	100	100	100	100
	98,6	98,6	99,1	100	100
	91,4	98,6	99,1	100	100
		96,6	98	96,6	98

**88.1 % connected**  
**0% shorts**

Connection (%)  [98-8] %  [8-0] %  
 Overall connection yield > 88,1 %  
 Overall Short circuit defects (<0,01%)

# Conclusion

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We demonstrated:

- Postprocessing technologies feasible on CMOS Chips (*tubes & solder lands*)
- Insertion technology feasible @ room temperature with 0.5 mN insertion force/ tube
- Encouraging yield for 4 millions connections @ 10 $\mu$ m pitch
- Vertical contact resistance < 1  $\Omega$  per connection (100 $\mu$ m<sup>2</sup>)
- Yield enhancement using autolevelling tools was effective

# Future work

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- Adapt process for 3D applications (*solder, tubes...*)
- Improve yield (*planarity, ...*)
- Improve access resistance (*intermetallics diffusion control*)
- Reduce connection pitch (*objective 5 $\mu$ m connection pitch*)

# Acknowledgement

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- CEA-LETI, Minatec and Carnot fundings
- Smart Equipment Technology (SET<sup>®</sup>)

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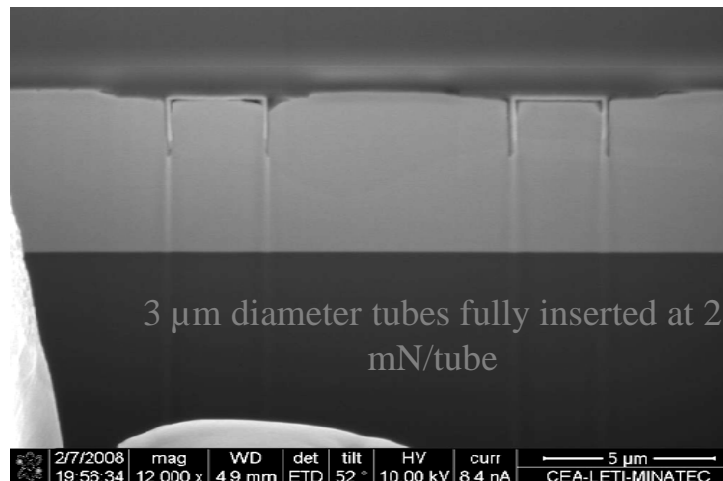
Thank you for your attention



# Process set up using full sheet solder layer

## ■ Results:

- Insertion depth (pull out force) depends on  $\mu$ tube diameter (Load=cst)
- Min load  $\in [0.3 ; 1]$  mN/ $\mu$ tube (depends on tube diameter)



# FIB analysis

*(Local)*  
Teos dep

