Chip to wafer copper direct bonding electrical characterization and thermal cycling

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***Abstract*—Copper direct bonding technology is considered to be one of the most promising approach for matching the miniaturization needs of future 3D integrated high performance circuits (3D-IC). In this study, we discuss the recent achievements in copper direct bonding technology with oxide/copper mixed surface and present the latest electrical and physical characterizations of chip to wafer bonding structures after annealing at 400°C and thermal cycling tests. In addition, electrical performance of chip to wafer bonding on 300mm wafers is also presented. Finally, thermo-mechanical finite element simulations showing the impact of the annealing conditions on the closure of the interface are shown.**

Keywords—3D integration; copper direct bonding; chip to wafer; electrical characterization; finite element simulations.

I. Introduction

Three-dimensional integration is considered as one of the most promising way to dramatically improve both the performance and the heterogeneity of electronic devices [1]. This technology consists in stacking several wafers or chips together to achieve high interconnection density while reducing their length. To obtain functional bonded devices, main key steps like surface preparation, alignment, bonding, thinning and Through Silicon Via (TSV) connections must be mastered. The two main bonding techniques allowing simultaneous mechanical and electrical connection are thermo-compression bonding [2, 3] and metallic direct bonding [4, 5, 6]. While both techniques have their advantages, copper direct bonding appears to be the most encouraging way to achieve very high interconnection density. Previous studies have demonstrated the relevance of the Wafer to Wafer (WtW) copper direct bonding technology with robust electrical performance on 200mm wafers [7]. Nevertheless, a WtW strategy entails significant drawbacks, such as a constant die footprint between tiers and the impossibility to ensure high production yields without prior Known Good Dies (KGD) selection. For these reasons, a Chip to Wafer (CtW) strategy has been carried out and assessed on 200mm and 300mm wafers environments, high density interconnects being generally required for advanced CMOS node. In this paper we present the latest electrical characterizations of 200mm CtW bonding after annealing at 400°C and Thermal Cycling (TC) tests, and we compare them to 200mm WtW bonding technology. In addition, electrical performances of 300mm CtW bonding were also investigated. Finally, thermo-mechanical finite element simulations were done to investigate different annealing conditions and their impact on the closure mechanism of the bonding interface.

II. Experiments

For previous studies, a test-vehicle (TV) was designed to allow the electrical characterization of WtW copper direct bonding with 200mm wafers [8]. This TV was then adapted to CtW bonding on both 200mm and 300mm wafers in order to proceed to further studies on CtW technology. In this case, the receiver wafer included distant contact pads, allowing to quickly characterize the bonding interface without any further technological steps. Copper direct bonding consists in a specific surface preparation process, including an optimized Chemical Mechanical Polishing (CMP) step resulting in a low total thickness variation, a very low surface roughness and a well-controlled copper dishing. While the bonding step is done at room temperature and ambient pressure, an annealing step could be necessary to increase the bonding strength between the chip and the wafer. Generally performed between 200°C and 400°C, this thermal treatment leads to the creation of covalent bonds at the silicon oxide interface and metallic bonds at the Cu-Cu interface, which strengthen the whole bonding interface [8, 9]. In this study, both WtW and CtW bonding were realized at room temperature, atmospheric pressure and ambient air, then annealed at 400°C. TC tests were based on a classical JEDEC standard (JESD22-A104D), with 1000 cycles and a temperature range between -40°C and +125°C. The face to face direct bonded structures are fully compatible with subsequent standard TSV processes and high density interconnection. The purpose of this work was then to compare electrical performances between WtW and CtW structures on 200mm wafer and to implement the CtW technology to the 300mm wafer platform. The following parts describe the test structures used to characterize the bonding interface and the integration processes of both 200mm WtW test-vehicle and 200mm/300mm CtW test-vehicles. All the resistance measurements were carried out by the 4-probe Kelvin measurement method on a Cascade Microtech™ 12000 manual prober.

A. *Experimental structures*

The two main structures used to characterize the electrical resistance of the Cu-Cu bonding interface were bonded and stand-alone NIST (National Institute of Standard Technology) and daisy chains structures. A schematic description of the bonded and stand-alone NIST structures can be found in the Fig. 1. The stand-alone NIST (d) were used to first extract the copper resistivity and then to calculate the theoretical resistance for the bonded structures. The contact area of these structures is 640 x 3µm² for the NIST (a) and (c), and 340 x 3µm² for the NIST (b). The probe pads of the NIST (a) and (b) are situated on two different layers, which forces the current to pass through the bonding interface during the electrical characterization. On the contrary, the contact pads of the bonded structure NIST (c) are on the same metal layer. Therefore, if the contact resistance is too high, in the case of a poor bonding quality for instance, the current would flow only in the upper line without crossing the bonding interface.

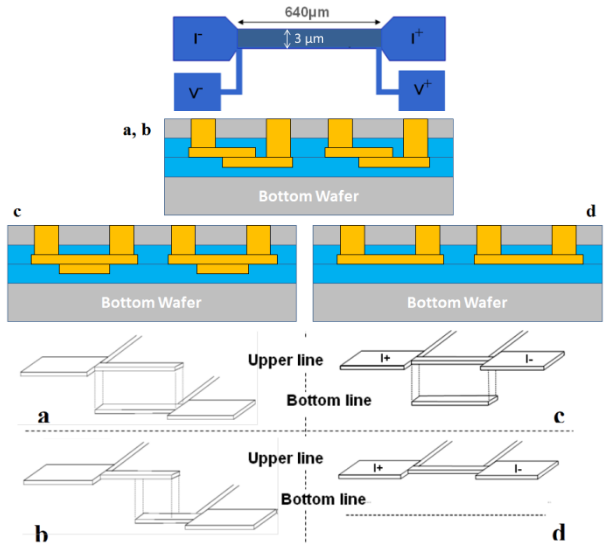


Fig 1. Top view and schematic diagram of the bonded (a, b & c) and stand-alone (d) NIST structures.

The daisy chain (DC) structures consist in long chains of interconnections between the top layer and the bottom layer, aimed at validating the compatibility of this direct bonding process with high density interconnections stacks (Fig. 2). Five different DC were characterized, each DC having a specific number of connections, contact area and pitch. The detailed characteristics of the five DC are summarized in the table I.

TABLE I. CHARACTERISTICS OF THE FIVE DAISY CHAINS

Daisy Chains	DC1	DC2	DC3	DC4	DC5
Connection number	10 136	4872	10 772	14 934	29 422
Contact area (µm²)	3 x 3	5 x 5	3 x 3	3 x 3	3 x 3
Pitch x / y (µm)	7 / 21	10 / 30	7 / 19	7 / 14	7 / 7

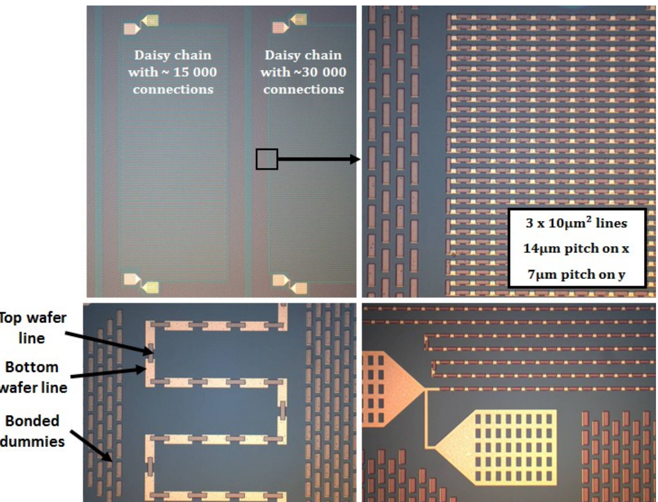


Fig 2. Top down optical observations of daisy chains after the complete removal of top silicon wafer.

B. *200mm wafer to wafer integration process*

The fabrication was performed at CEA Leti on 200mm silicon wafers, based on a classical damascene process. After 500nm thick opening into an 800nm thick deposited SiO_2 layer, TiN diffusion barrier and Cu seed layers were deposited. Cu filling was carried out by electroplating and then annealed at 400°C. After an optimized CMP surface preparation, wafers were bonded at room temperature, atmospheric pressure and ambient air. In order to strengthen the bonding interface, the stacked wafers were annealed at 400°C during 2 hours. To allow the direct probing at a wafer level, several technological steps are performed on the bounded wafers: top wafer thinning down to 50µm, via etching and realization of a redistribution layer (RDL). Finally, a BCB passivation and a UBM layers were processed (Fig. 3).

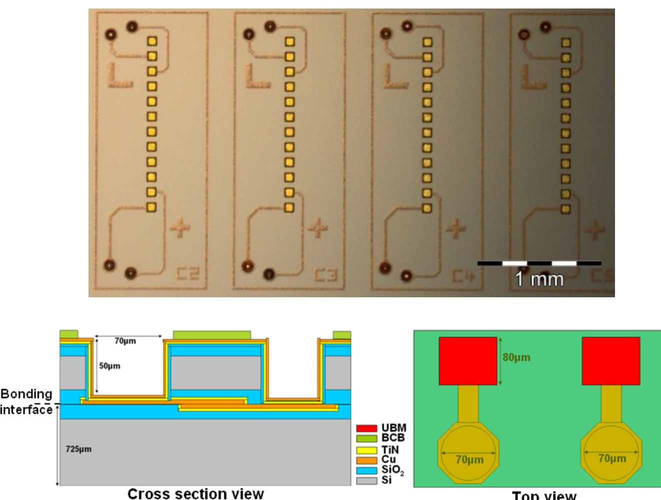


Fig 3. Top view and schematic diagram of the full integration used for wafer level electrical tests.

C. *200mm & 300mm chip to wafer integration process*

The bottom wafer on which the chips were bonded was designed to integrate distant contact pads, allowing to quickly

characterize the bonding interface without any further steps of lithography and etching. The fabrication process of the 200mm wafer is the same as the WtW bonding. However, the metallization of 300mm wafers is composed by a TaN/Ta diffusion barrier and a copper from STMicroelectronics Crolles fab. The 200mm top wafers were diced after the optimized damascene-like CMP surface preparation to obtain 1cm² chips. The SET FC300 pick & place machine, along with a collective surface preparation process, was used to perform the CtW bonding on 200mm and 300mm wafers, with an alignment accuracy between 0.2µm and 1µm (Fig. 4).

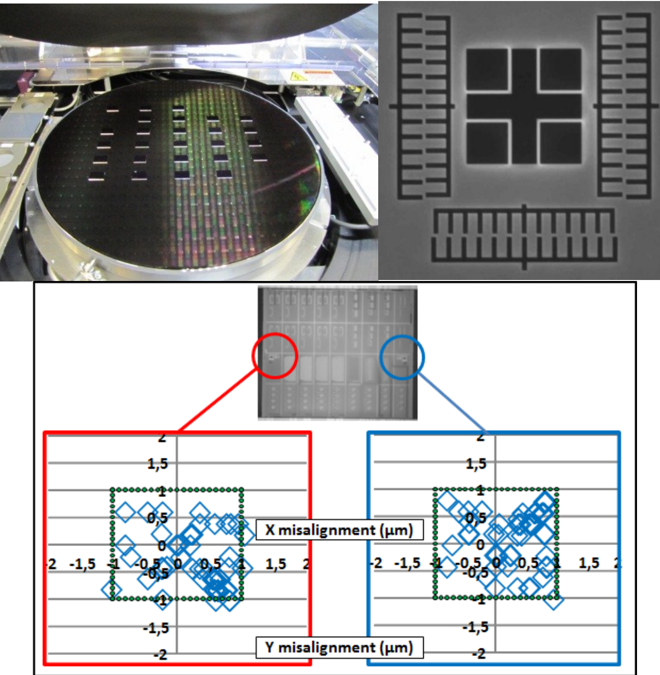


Fig 4. Top left: Bonded chips on a 300mm wafer. Top Right: Example of infrared microscope image of cross-in-box and verniers at the bonding interface used for high precision measurements. Bottom: Chip to wafer misalignment in both x and y directions, measured on the left and right alignment patterns of 50 chips.

Finally, a post-bonding wafer level SiN encapsulation was required before the 400°C annealing step to prevent further oxidation of the copper. The final integration and the location of the test probes are represented in the schematics in the Fig. 5.

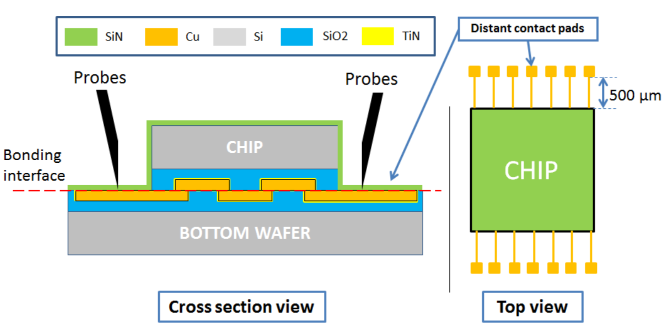


Fig 5. Schematic diagrams of a bonded chip with electrical characterization probes (left) in contact with the deported pads 500µm away from the top chip (right).

The Fig. 6 shows an optical image and an infrared characterization of one of the 41 chips that were bonded and electrically tested. This infrared inspection shows a very good bonding quality after bonding as no interference fringe or particle is visible on the chip.

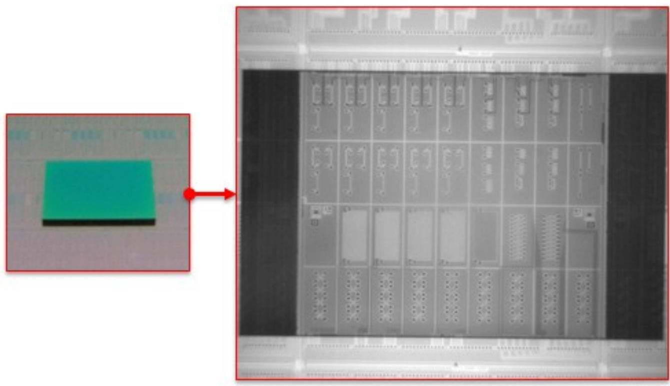


Fig 6. Optical and infrared images of a 200mm chip to wafer bonding done for this study.

III. Electrical Results and Discussion

A. 200mm wafer to wafer vs chip to wafer bonding

Stand-alone NIST (d) structures were used to extract a reference value for copper resistivity on the WtW and CtW bonding. Copper line resistance was measured with a 4-probe electrical characterization on NIST structures. The equation used to extract the resistivity from the resistance and the structures geometry is:

$$\rho = (R \times S) / L$$

Where R is the measured copper line resistance, L the copper line length (L = 640µm) and S its section (S = 3 x 0.5µm²). The copper resistivity for the WtW bonding and the CtW bonding was $\rho = 2.01.10^{-2}\Omega.\mu m$. The following tables II and III compile the structure characteristics, the theoretical resistances and the experimental resistances for all the NIST structures.

TABLE II. Resistances of bonded and stand-alone NIST (200mm)

				Copper Resistivity
NIST Structures	**NIST a**	**NIST b**	**NIST c**	**NIST d**
Contact Area (µm²)	640 x 3	340 x 3	640 x 3	$\rho = 2.10^{-2}\ \Omega.\mu m$
Theoretical Res. (Ω)	4.27	6.26	4.27	
Wafer to Wafer (200mm)				
Experimental Res. (Ω)	4.39	6.34	4.31	8.53
Chip to Wafer (200mm)				
Experimental Res. (Ω)	4.52	6.37	4.47	8.58

In the table II we present a comparison between 200mm WtW and CtW experimental resistance along with theoretical resistance calculated thanks to the extracted resistivity. As already shown by Taibi *et al* [7], WtW structures are in very good accordance with the theoretical values. Furthermore, the

bonding interface offers a very low resistance since the results between NIST (a) and NIST (c) are very close, showing that the current passes through the entire bonded line, even if it is not forced to do so in the case of the NIST (c). In addition, the same behavior is observed on the CtW structures. Indeed, the electrical resistances are very close to both the theoretical resistance and the WtW structures, showing a very good bonding quality of the copper and a low resistance interface.

TABLE III. RESISTANCES OF DAISY CHAINS (200MM)

Daisy Chains	DC1	DC2	DC3	DC4	DC5
Connection number	10 136	4872	10 772	14 934	29 422
Contact area (µm²)	3 x 3	5 x 5	3 x 3	3 x 3	3 x 3
Pitch x / y (µm)	7 / 21	10 / 30	7 / 19	7 / 14	7 / 7
Theoretical Res. (Ω)	780.5	304	624.8	1149.9	2265.5
Th. Res. per node (mΩ)	77	62.4	58	77	77
Wafer to Wafer (200mm)					
Global resistance (Ω)	801	310	681	1180	2340
Res. per node (mΩ)	79	63.6	63.2	79	79.5
Chip to Wafer (200mm)					
Global resistance (Ω)	793	304	661	1160	2297
Res. per node (mΩ)	78.2	62.4	61.3	77.6	78

The table III presents theoretical and experimental electrical resistance of the five DC for both WtW and CtW on 200mm wafers. By calculating the theoretical resistance of a node using the extracted resistivity and the equivalent circuit shown in the Fig. 7, we can predict the global resistance of the daisy chain by multiplying this theoretical resistance of a node by the number of connections.

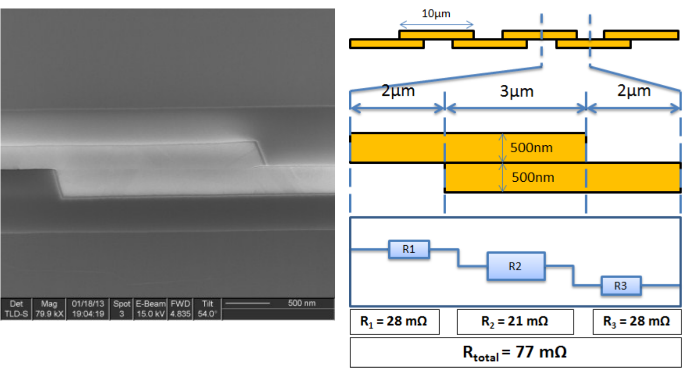
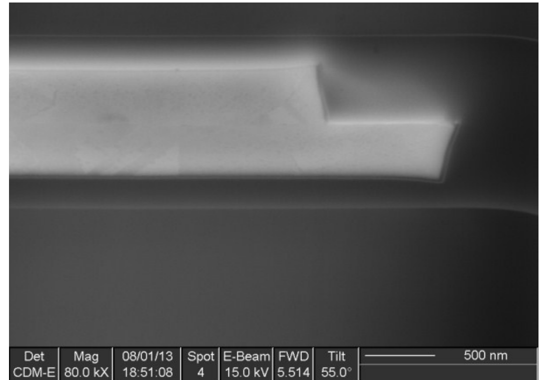


Fig 7. SEM picture, schematic view and equivalent circuit of the DC5 daisy chain node. Because the copper lines of the wafer and the chip have the same resistivity, the equivalent circuit chosen to model the node is simply a series of resistors.

The difference between experimental and theoretical resistance for the CtW DC5 node is only 1mΩ, which is significantly lower than the 2.5mΩ of the WtW DC5 node. This difference could be attributed to variations in the fabrication process, a better bonding quality and a robust alignment between the chip and the wafer. These results globally confirm the very good bonding quality of the CtW process as well as the absence of impact on the electrical performances compare to the WtW process. Furthermore, it strongly validates the CtW technology as a reproducible method to realize high interconnection density 3DIC.

Chip to wafer bonding offers a lot of advantages from design and integration points of view, but various questions about the mechanical strength or the reliability of the stacks must be investigated. This is why we conducted for the first time thermal cycling tests on non-thinned CtW bonding structures, based on a classical JEDEC standard with 1000 cycles at ambient pressure and a temperature cycling between -40°C and +125°C. In order to verify the structural integrity of the interface, electrical characterizations and SEM images were realized after the TC tests. As shown on the Fig. 8, no increase of the resistance or dramatic failure caused by major structural deformations, like voids or delamination, was observed on the NIST and daisy chain structures. This encouraging result indicates the high mechanical strength of non-thinned bonded chips, but in order to fully address the mechanical reliability question of CtW stacks, additional investigations must be conducted in the future, including TC tests on thinned-down chips with a complete BEOL and thermo-mechanical simulations.



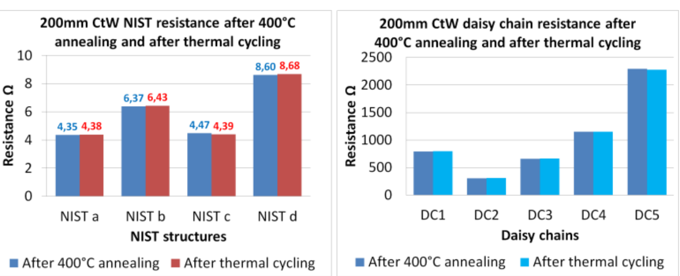


Fig 8. Top: SEM image of the right edge of a CtW 3µm wide NIST line after thermal cycling test. Bottom: Electrical resistance comparison between NIST (left) and daisy chains (right) annealed at 400°C and submitted to a thermal cycling test.

B. 300mm chip to wafer bonding

The copper lines on the 300mm wafer are 500nm high and have a 25nm high TaN/Ta diffusion barrier, while the copper lines on the chips are 350nm high and have a 20nm high TiN diffusion barrier. Also, variations in the deposition conditions induce a slight difference in the grain sizes of the copper line. Thus, the extracted copper resistivity were $\rho_{chip} = 2.16.10^{-2}\Omega.\mu m$ for the chip and $\rho_{wafer} = 2.13.10^{-2}\Omega.\mu m$ for the wafer, which is slightly higher than the resistivity found on the 200mm CtW bonding. Nevertheless, the experimental

resistances for the NIST and daisy chain structures on the 300mm CtW bonding are in very good accordance with the theoretical values. All the structure characteristics, the theoretical resistance and the experimental resistance are compiled in the following tables IV and V.

TABLE IV. RESISTANCES OF BONDED AND STAND-ALONE NIST (300MM)

NIST Structures	NIST a	NIST b	NIST c	Copper resistivity NIST d	 NIST e
Contact Area (µm²)	640 x 3	340 x 3	640 x 3	ρ = 2.16.10⁻² Ω.µm	ρ = 2.13.10⁻² Ω.µm
Theoretical Res. (Ω)	5.38	8.07	5.38		
Experimental Res. (Ω)	5.50	8.08	5.60	13.3	9.31

TABLE V. RESISTANCES OF DAISY CHAINS (300MM)

Daisy Chains	DC1	DC2	DC3	DC4	DC5
Connection number	10 136	4872	10 772	14 934	29 422
Contact area (µm²)	3 x 3	5 x 5	3 x 3	3 x 3	3 x 3
Pitch x / y (µm)	7 / 21	10 / 30	7 / 19	7 / 14	7 / 7
Theoretical Res. (Ω)	959.88	377.09	785.3	1414.25	2786.26
Th. Res. per node (mΩ)	94.7	77.4	72.9	94.7	94.7
Global resistance (Ω)	997.9	384.4	830.8	1488.8	2914.6
Res. per node (mΩ)	98.4	78.9	77.1	99.7	99

The table V presents theoretical and experimental electrical resistance of the five daisy chain structures. The difference of resistivity between the copper lines of the top chips and the bottom wafer led us to choose another equivalent circuit to calculate the theoretical resistance of the daisy chain nodes. This time we considered two resistors $R2_t$ and $R2_b$ in parallel to model the bonded part of the node. The total resistance R2 is defined by the following equation:

$$R2 = \frac{1}{\frac{1}{R2_t} + \frac{1}{R2_b}}$$

The figure 9 details the calculation of the theoretical resistance for the DC5 daisy chain node:

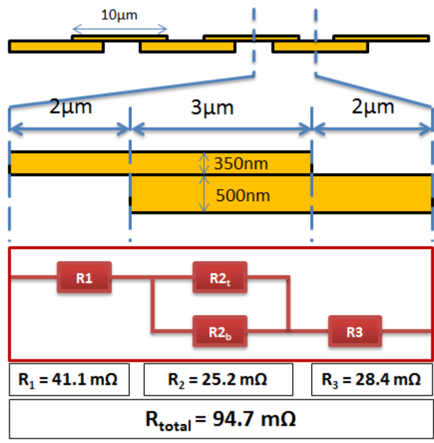


Fig 9. Schematic view and equivalent circuit of the DC5 daisy chain node.

The difference between experimental and theoretical resistance for the DC5 node is 4.7mΩ this time, which proves a robust bonding quality, the bonding interface having little impact on the global resistance. This result is all the more interesting as the bonded samples come from two different technologies, demonstrating the feasibility of heterogeneous integration with the direct bonding technology. Moreover, by comparing the resistances of all the NIST present on the 19 bonded chips, we did not notice any significant variations (Fig. 10). Indeed, the standard deviation for the NIST (a) and (b) is 3.39% and 1.47% respectively, which is in accordance with industry standards regarding interconnections. This result implies high fabrication homogeneity and confirms that the CtW bonding process gives good electrical performances whether the chip is bonded on the edge or at the center of the 300mm wafer.

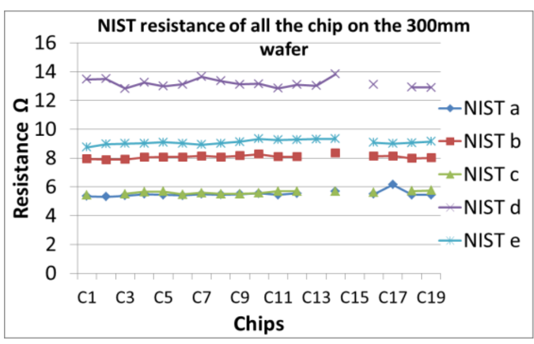


Fig 10. Resistances of all the NIST structures present on the 19 chips bonded on the 300mm wafer. No impact of the position of the chip on the electrical performance is noticeable.

IV. FINITE ELEMENT SIMULATIONS: IMPACT OF ANNEALING CONDITIONS ON THE BONDING INTERFACE

In previous works [6], it has been already demonstrated that the copper to copper adhesion is driven by the copper expansion upon annealing. Thus, modeling the adhesion, expansion and local strain mechanisms between two copper pads is of main concern to understand the reliability and failure modes of such an electrical interconnection. To this purpose, two dimensional thermo-mechanical finite element simulations were conducted with Abaqus tool to better understand these mechanisms. Under thermal treatment, the SiO2/SiO2 interface strengthens, increasing the bonding energy, and the copper lines expand vertically. This is why the dishing effect of the copper has to be very well controlled so that the interface properly closes during annealing. These simulations should help us determine some design rules regarding the maximum authorized dishing for a particular copper line shape.

In this particular study, we present the first results concerning the impact of the annealing conditions on 3µm wide 500nm thick bonded copper lines with a 20nm copper dishing (Fig. 11). The simulations were carried out in two dimensions and the whole structure was considered under plane stress, given that the length of the line in the Z direction is very large compare to its width and its thickness. The parameters describing the elastic-plastic behavior of the copper, expressed in TPa as the parts dimensions are micrometric, are summarized in the following table VI:

TABLE VI. PHYSICAL PARAMETERS OF THE SIMULATED COPPER

Property	Symbol	Value
Young's Modulus	E	0.12 TPa
Poisson's Ratio	ν	0.34
Expansion Coeff	α	$1.65*10^{-5}\ K^{-1}$
Yield Stress	R_0	$180*10^{-6}$ TPa
Kinetic Hardening	C	0.6026 TPa
Gamma 1	γ	2300
Q-infinity	Q	$30*10^{-5}$ TPa
Hardening Param	b	100

Concerning the boundary conditions, the bottom edge of the bottom part was considered fixed during all the calculation. Symmetry along the X axis was chosen for the side edges of both parts. Finally, in order to evaluate the impact of the annealing conditions on the bonding interface, we considered two different case studies using different boundary conditions for the top edge of the top part. In the first case the top wafer is free to move along the Y axis, while in the second case the top edge is pinned. A 500nm misalignment between the two copper lines was introduced to correspond to typical alignment precision offered by current bonding machines.

The simulation scenario was divided into 3 main steps. The first one consisted in the approach of the top part toward the bottom one, initially separated from 1µm, in order to initiate the bonding at ambient temperature. During the second step the annealing at 400°C occurred, which led to the copper dilatation and thus the complete or partial closure of the copper interface. Finally during the last step the parts assembly cooled down, going from 400°C to 20°C.

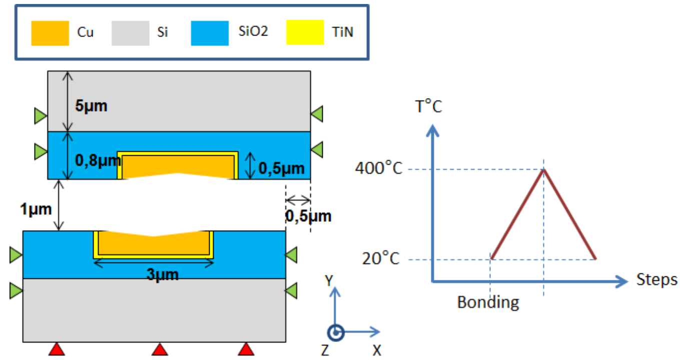


Fig 11. Schematic view of the parts, general boundary conditions and simulation scenario.

A user subroutine was implemented to take into account the cohesive interactions occurring at the SiO_2/SiO_2 and Cu/Cu interfaces. The equations of this cohesive model are based on the exponential cohesive zone law, which uses potential energy and was originally proposed by X. P. Xu and A. Needleman [10] (Fig. 12). The exponential potential is expressed as:

$$\Psi(\Delta_n, \Delta_t) = \phi_n + \phi_n \exp\left(\frac{-\Delta_n}{\delta_n}\right)\left\{\left[1 - r + \frac{\Delta_n}{\delta_n}\right]\frac{(1-q)}{(r-1)} - \left[q + \frac{(r-q)}{(r-1)}\frac{\Delta_n}{\delta_n}\right]\exp\left(-\frac{\Delta_t^2}{\delta_t^2}\right)\right\} \quad (1)$$

Where Δ_n is a normal separation variable, $q = \varphi_t / \varphi_n$ and $r = \Delta_n^* / \delta_n$, Δ_n^* being the value of Δ_n after complete shear separation under the condition of zero normal tension, i.e., $T_n = 0$. δ_n and δ_t are normal and tangential characteristic lengths associated with the mode I fracture energy φ_n, the mode II fracture energy φ_t, the tangential cohesive strength τ_{max}, and the normal cohesive strength σ_{max}:

$$\phi_n = \sigma_{\max} e \delta_n, \quad \phi_t = \sqrt{e/2}\,\tau_{\max}\delta_t$$

For these particular simulations, we chose the case where q = 1 and r = 0. In these conditions, the potential is defined as:

$$\Psi(\Delta_n, \Delta_t) = \phi_n - \phi_n\left[1 + \frac{\Delta_n}{\delta_n}\right]\exp\left(\frac{-\Delta_n}{\delta_n}\right)\exp\left(-\frac{\Delta_t^2}{\delta_t^2}\right) \quad (2)$$

Previous studies have evaluated the bonding energy at ambient temperature of oxide/copper mixed surface to about 750mJ/m² [9]. Because of the two dimensional nature of our model and the chosen boundary conditions, we considered that the normal interactions were predominant on the tangential ones. This way, we only used the mode I fracture energy φ_n to estimate the σ_{max} and δ_n parameter values to 280MPa and 1nm respectively, which gives:

$$\varphi_n = 280.10^6 * \exp(1) * 1.10^{-9} = 756\text{mJ/m}^2$$

To simulate the strength increase of the bonding interface under thermal treatment, the σ_{max} parameter was dynamically increased during the annealing step of the calculation. The cohesive force being increased that way, the separation of the bonded interface due to the shrinking of the copper line during the stage of cooling does not occur.

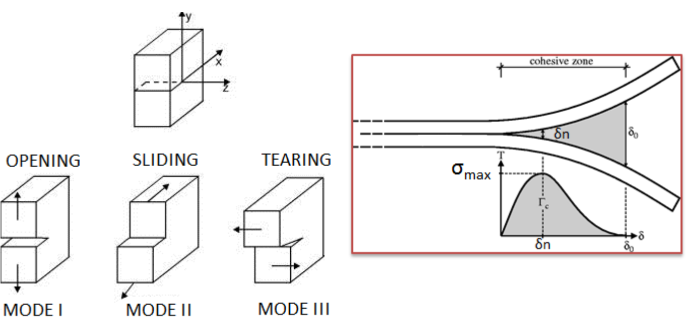


Fig 12. Schematic view of the different fracture modes and the cohesive zone model employed in this study.

The Fig. 13 offers a comparison of the state of both case studies at the final step of the computation. The color scale represents the vertical stress in TPa. We can clearly see a huge difference in the closure state between the two case studies. Indeed, in the first case the copper interface is partially closed, indicating that the copper line was able to retract during the cooling step. However, we can notice that the copper interface is bonded at the extremities of the line, which implies a tensile stress of about 0.7MPa throughout the thickness of the line. The maximum tensile stress is situated at the TiN/Cu interface and is about 300MPa. In the second case study, the copper interface is completely closed and an important tensile stress is noticeable, going from about 10MPa at the center of the line, to

1GPa at the edge of the line. This tension is the result of the competition between the shrinkage of the copper and the bonding strength of the interface. Indeed, during the cooling stage of the computation, the copper tends to shrink but in this case the bonding strength keeps the interface closed, causing the tensile stress to increase. The boundary conditions used for this second case study seem to favor the closure of the copper interface because the expansion of the top wafer is forced downwards. These first results tend to indicate that, by applying a constant pressure on the top wafer during the annealing at 400°C, it would be possible to completely bond two copper lines usually impossible to bond under thermal treatment due to an excessive dishing effect. However, in order to predict and prevent preferential failure mechanisms, the distribution of the stress and its magnitude should be further investigated, by taking into account the creep phenomenon for example.

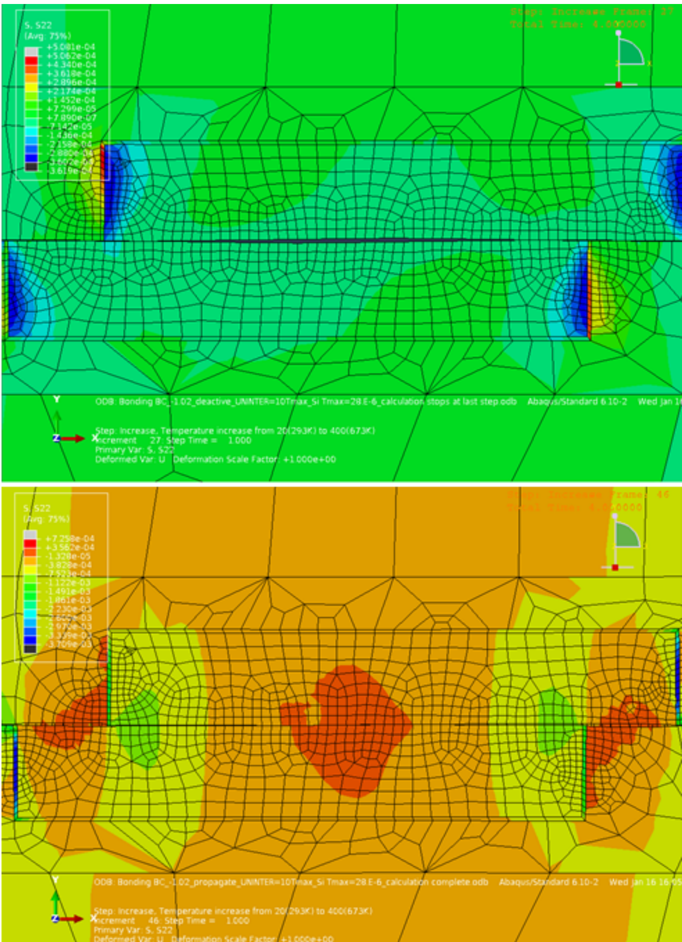


Fig 13. Top, fist case study: Simulation results of a 3µm wide bonded copper line with a 20nm dishing, after annealing at 400°C. The top wafer is free to move along the Y axis. Bottom, second case study: Simulation results of a 3µm wide bonded copper line with a 20nm dishing, after annealing at 400°C. The top edge of the top wafer is pinned.

V. Conclusions

In this paper, we presented and discussed the recent achievements in transferring the 200mm wafer level direct Cu-Cu bonding to 200mm and 300mm chip to wafer processes. By comparing with the previous electrical results obtained on 200mm wafer to wafer bonding, we showed that the chip to wafer technology offers equivalent electrical performances along with a very satisfying homogeneity. Furthermore, the very good concordance between the theoretical and the experimental resistance, especially concerning the daisy chain with more than 30 000 interconnections, along with the fact that the chip's position on the wafer has no impact on the electrical performance, validates the CtW process as a reproducible and promising manner to realize high density three-dimensional integrated circuits. In order to better understand the closure mechanisms of the copper interface, two dimensional thermo-mechanical finite element simulations have been presented. The first results indicate that it could be possible to compensate a large dishing effect of the copper line by applying a constant pressure on the top wafer during the annealing step.

Acknowledgment

This work was funded thanks to the French national program "Programme d'Investissements d'Avenir, IRT Nanoelec" ANR-10-AIRT-05.

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