

# Results of the 2015 testbeam of a 180 nm AMS High-Voltage CMOS sensor prototype

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**M. Benoit<sup>a</sup>, J. Bilbao de Mendizabal<sup>a</sup>, G. Casse<sup>b</sup>, H. Chen<sup>c</sup>, K. Chen<sup>c</sup>, F.A. Di Bello<sup>a,1</sup>, D. Ferrere<sup>a</sup>, T. Golling<sup>a</sup>, S. Gonzalez-Sevilla<sup>a,1</sup>, G. Iacobucci<sup>a</sup>, F. Lanni<sup>c</sup>, H. Liu<sup>c,d</sup>, F. Meloni<sup>e</sup>, L. Meng<sup>a,b</sup>, A. Miucci<sup>a,2</sup>, D. Muenstermann<sup>a,3</sup>, M. Nessi<sup>a,f</sup>, I. Perić<sup>g</sup>, M. Rimoldi<sup>e</sup>, B. Ristic<sup>a,f</sup>, M. Vicente Barrero Pinto<sup>a</sup>, J. Vosseveld<sup>b</sup>, M. Weber<sup>e</sup>, W. Wu<sup>c</sup>, and L. Xu<sup>c</sup>**

<sup>a</sup>*Département de Physique Nucléaire et Corpusculaire (DPNC), University of Geneva, 24 quai Ernest Ansermet 1211 Genève 4, Switzerland*

<sup>b</sup>*Department of Physics, University of Liverpool, The Oliver Lodge Laboratory, Liverpool L69 7ZE, UK*

<sup>c</sup>*Brookhaven National Laboratory (BNL), P.O. Box 5000, Upton, NY 11973-5000, USA*

<sup>d</sup>*Department of Modern Physics, University of Science and Technology of China, Hefei, Anhui 230026, China*

<sup>e</sup>*Albert Einstein Center for Fundamental Physics and Laboratory for High Energy Physics, University of Bern, Sidlerstrasse 5, CH-3012 Bern, Switzerland*

<sup>f</sup>*European Organization for Nuclear Research (CERN), 385 route de Meyrin, 1217 Meyrin, Switzerland*

<sup>g</sup>*Karlsruhe Institute of Technology (KIT), Kaiserstraße 12, 76131 Karlsruhe, Germany*

*E-mail:* Sergio.Gonzalez@unige.ch

**ABSTRACT:** Active pixel sensors based on the High-Voltage CMOS technology are being investigated as a viable option for the future pixel tracker of the ATLAS experiment at the High-Luminosity LHC. This paper reports on the testbeam measurements performed at the H8 beamline of the CERN Super Proton Synchrotron on a High-Voltage CMOS sensor prototype produced in 180 nm AMS technology. Results in terms of tracking efficiency and timing performance, for different threshold and bias conditions, are shown.

**KEYWORDS:** Solid state detectors, Si microstrip and pad detectors, Particle tracking detectors, Electronic detector readout concepts, Performance of High Energy Physics Detectors.

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<sup>1</sup>Corresponding author

<sup>2</sup>Now at Albert Einstein Center for Fundamental Physics and Laboratory for High Energy Physics, University of Bern, Sidlerstrasse 5, CH-3012 Bern, Switzerland

<sup>3</sup>Now at Physics Department, Lancaster University, Lancaster, UK, LA1 4YB.

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## 1. Introduction

Active pixel sensors based on the High-Voltage CMOS (HV-CMOS) technology [1] are promising candidates for the next generation of pixel tracking detectors in High Energy Physics experiments. The operating principle is based on a thin  $p$ -type silicon bulk containing a deep  $n$ -well that implements CMOS pixel electronics (*e.g.* preamplifier, discriminator). A reverse bias voltage is applied to the diode formed by  $n$ -well with respect to the substrate to create a depletion region. The charge carriers, created by ionization, drift towards the  $n$ -well that acts as a collecting electrode. As the transistors are physically isolated from the substrate, a relatively high bias voltage ( $\sim 100$  V) can be applied to enlarge the depletion zone. A readout ASIC coupled to the HV-CMOS sensor is used to collect the signal and perform further digital processing.

This paper reports on the testbeam results obtained for a HV-CMOS sensor prototype produced in 180 nm technology by ams AG [2] (AMS). This manuscript is organized as follows. Section 2 describes the experimental setup and the telescope used for track reconstruction. Section 3 describes the Device Under Test (DUT). The offline analysis framework is briefly explained in Sec. 4. Finally, Sec. 5 presents the main results.

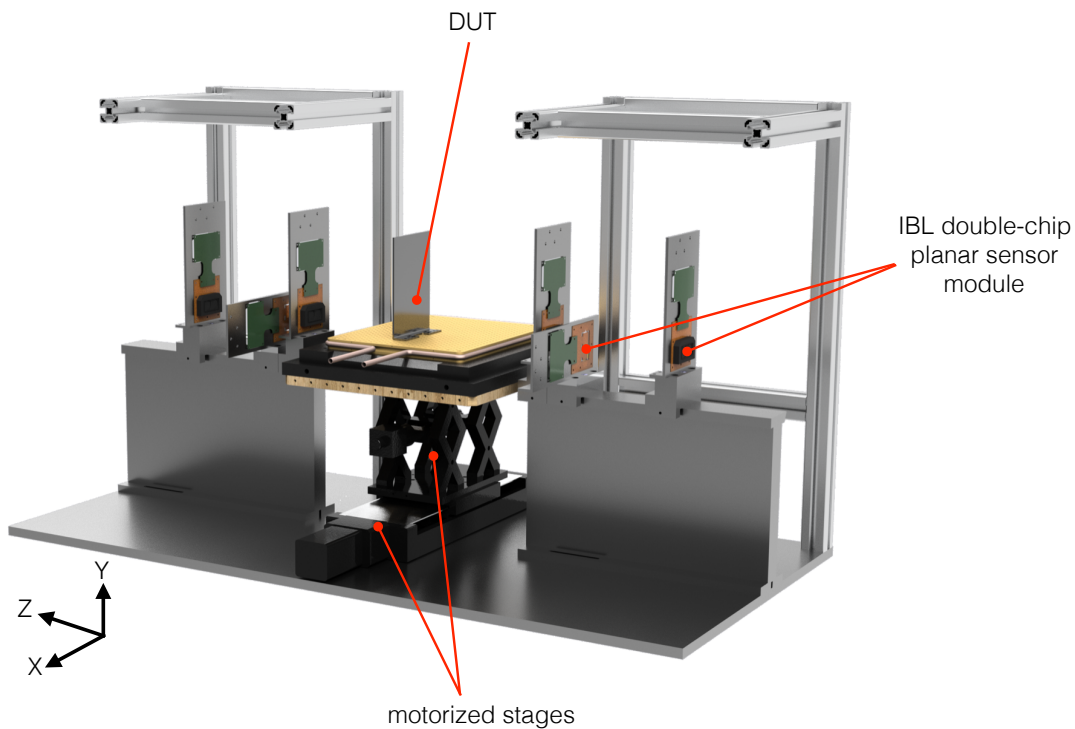


Figure 1: A rendered view of the FE-I4 beam telescope. The coordinate system is defined with the Z-axis along the beam-axis, the Y-axis pointing vertically upwards and the X-axis pointing horizontally.

## 2. Experimental setup

The AMS HV-CMOS detector prototype was tested in November 2015 at the H8 beamline of the CERN Super Proton Synchrotron (SPS), that provided a 180 GeV  $\pi^+$  beam. A dedicated beam telescope (hereafter called FE-I4 telescope) was used to provide a standalone measurement of the trajectories of the incoming particles independently of the device under test.

### 2.1 The FE-I4 beam telescope

The FE-I4 telescope [3] consists of six ATLAS Insertable B-Layer (IBL) [4] double-chip (DC) pixel modules [5] arranged in two arms of three modules each (see Fig. 1). Within a given arm, the first and last planes are installed vertically, with the most precise pixel coordinate ( $50\ \mu\text{m}$ -pitch, see below) along the Y-axis. The module in the middle is rotated by  $90^\circ$  to improve the spatial resolution along the X-direction.

Each DC module uses a  $200\ \mu\text{m}$ -thick  $n^+$ -in- $n$  planar silicon sensor produced by CiS [6]. The detector is segmented in a matrix of  $336\ \text{rows} \times 160\ \text{columns}$  with a pixel size of  $50 \times 250\ \mu\text{m}^2$ . The  $p^+$  back-side implant used for the high-voltage bias is surrounded by 13 guard rings shifted under the edge pixels, with a resulting total inactive area of only  $200\ \mu\text{m}$  from the sensor edge. Two FE-I4B [7] ASICs produced in IBM 130 nm CMOS technology are bump-bonded to the detector for the signal readout. Although the sensor can be readout by two ASICs, only one of them

was active during data-taking. The chip active area of  $20.2 \times 16.8 \text{ mm}^2$  holds 26'880 identical  $50 \times 250 \text{ }\mu\text{m}^2$  pixels organized in a matrix of 336 rows  $\times$  80 columns. Each pixel cell contains a two-stage amplifier followed by a discriminator with adjustable threshold, so that collected charge is translated into a 4-bit Time-over-Threshold (ToT) value measured in units of 25 ns (Bunch Crossing units or BC, corresponding to the LHC bunch spacing). The digital architecture is implemented such that four analog pixels share one common logic cell. The hit information is stored locally at the pixel level until reception of a trigger signal. For test and calibration purposes, a test charge with selectable amplitude can be directly injected into each pixel pre-amplifier input. A threshold tuning Digital-to-Analog Converter (DAC) is used to apply a per-pixel threshold correction. At this testbeam, the discriminator thresholds of the telescope modules FEs were tuned to a charge of  $2 \text{ ke}^-$ , with a final threshold dispersion of  $70 \text{ e}^-$ . The ToT to charge conversion was tuned for each pixel to 9 ToT units for a deposited charge of  $16 \text{ ke}^-$ .

## 2.2 Data Acquisition System

The Data Acquisition System (DAQ) of the FE-I4 telescope is based on the Reconfigurable Cluster Element (RCE), a generic computational element for DAQ systems developed at SLAC and based on System-on-Chip (SoC) technology. An Advanced Telecommunication Computing Architecture (ATCA) crate integrates several RCEs that are connected via optical links to a High Speed Input/Output (HSIO) development platform. The HSIO is a custom-made board based on the Xilinx Virtex-4 [8] FPGA developed by SLAC as a generic DAQ interface for both ATLAS Pixel and Strip detectors.

## 2.3 Trigger

The FE-I4B ASIC can provide a *HitBus* signal corresponding to the logical OR of selected pixel discriminator outputs. In the testbeam, the trigger signal for event acquisition is given by the coincidence (within one BC) of the *HitBus* signals of the first and last telescope modules. A pixel mask applied to the FE-I4B allows a precise definition of a Region-Of-Interest (ROI) on the triggering planes. By setting the ROI size to slightly exceed that of the device under test the data acquisition rate is optimized. A trigger rate of  $\sim 18 \text{ kHz}$  has been measured with the telescope in standalone mode (without DUT), and of  $\sim 6 \text{ kHz}$  with up to two FE-I4-based DUTs [3].

## 3. Device under test

The DUT, referred as AMS180v4, is the fourth version of a series of prototypes produced in the HV-CMOS technology by the AMS foundry. The AMS180v4 has been produced in 180 nm with the AMS H18 process. The unit cell structure contains six pixels arranged in two columns and three rows, each pixel having an area of  $125 \times 33 \text{ }\mu\text{m}^2$ . The substrate resistivity is  $20 \text{ }\Omega \cdot \text{cm}$ . The sensor (see Fig. 2a) has a total size of  $\sim 2.4 \times 2.9 \text{ mm}^2$ , a thickness of  $250 \text{ }\mu\text{m}$  and it implements various pixel types. The results presented in this paper correspond to the baseline flavour, so-called *STime*, where each pixel implements a two-stage amplifier followed by a discriminator with tuneable output amplitude. Though the discriminator threshold is common to all pixels in the sensor, a 4-bit DAC (TuneDAC or TDAC) is used to provide a per-pixel threshold dispersion correction.

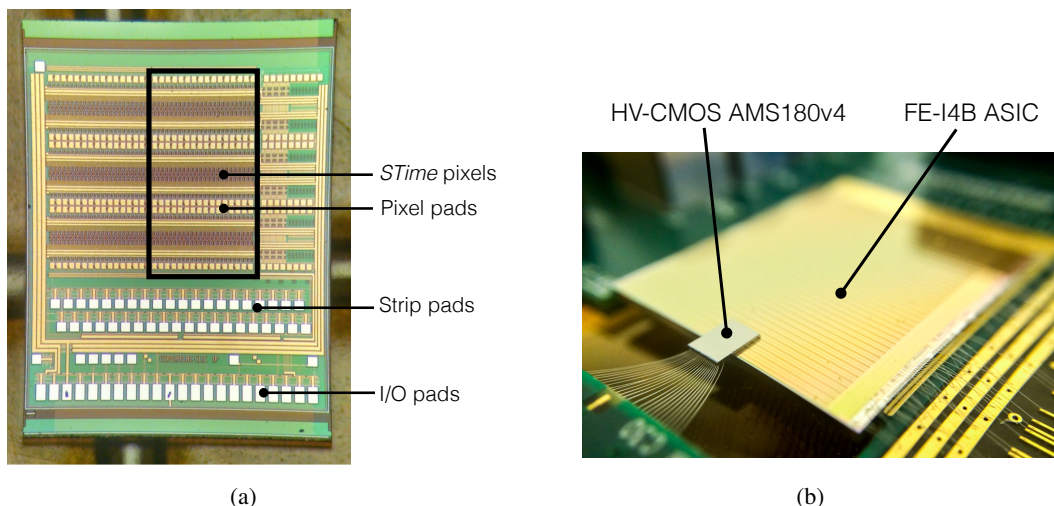


Figure 2: (a) AMS HV-CMOS 180 nm (version 4) bare sensor. The *I/O pads* are used to supply different analog voltages, the high-voltage bias and the digital inputs for the serial register configuration. The *Strip pads* were unused (these are needed only when operating the sensor with a strip readout chip). The *Pixel pads* have the same pitch as the FE-I4B pixels. (b) Final assembly of a FE-I4B pixel readout chip to a HV-CMOS v4 sensor via capacitive coupling.

The sensor has been designed to be compatible with either a pixel or a strip readout chip. For this measurement, a FE-I4B pixel readout ASIC was capacitively coupled to the HV-CMOS sensor by means of a  $< 1 \mu\text{m}$ -thick epoxy glue layer (see Fig. 2b). The SET ACC $\mu$ RA 100 flip-chip bonder [9] was used to bond the assembly with a post-bonding accuracy of  $1 \mu\text{m}$  and good coplanarity (maximum deviation of  $100 \text{ nm}$  over a total length of  $2.9 \text{ mm}$ ). After assembly, both the HV-CMOS sensor and the FE-I4B ASICs are wire-bonded to auxiliary boards (see section 3.2), providing all input voltages and control lines for both ICs.

As the FE-I4B pixel size is  $250 \times 50 \mu\text{m}^2$ , the unit cell, made by six HV-CMOS pixels, corresponds to two FE-I4 pixels (see Fig. 3). In this respect, we define *macro-pixel* as the set of three HV-CMOS single pixels (half the unit-cell) connected to a single FE-I4B readout pixel. For simplicity of operation in the testbeam, the signal amplitude of the discriminator output of each of these three sub-pixels were set to the same voltage level.

### 3.1 Charge calibration

In order to perform a voltage-to-charge calibration, a setup with a  $^{55}\text{Fe}$  radioactive source was used. The most intense emission of this X-ray source is at  $5.9 \text{ keV}$  ( $K_{\alpha}$  peak). Photons are absorbed in the silicon bulk creating photoelectrons that can then be collected. The  $^{55}\text{Fe}$  spectrum was recorded by monitoring with an oscilloscope the output signal of a single pixel after the amplification stage. The measurement was performed at room temperature with the sensor biased at  $80 \text{ V}$ . In order to estimate the intrinsic noise level of the setup, a first acquisition without the source was performed. The threshold of the oscilloscope was then set at five times the r.m.s. of the (Gaussian-distributed) noise distribution. By determining the position of the  $K_{\alpha}$  peak and assuming  $3.65 \text{ eV}$  as the ioniza-

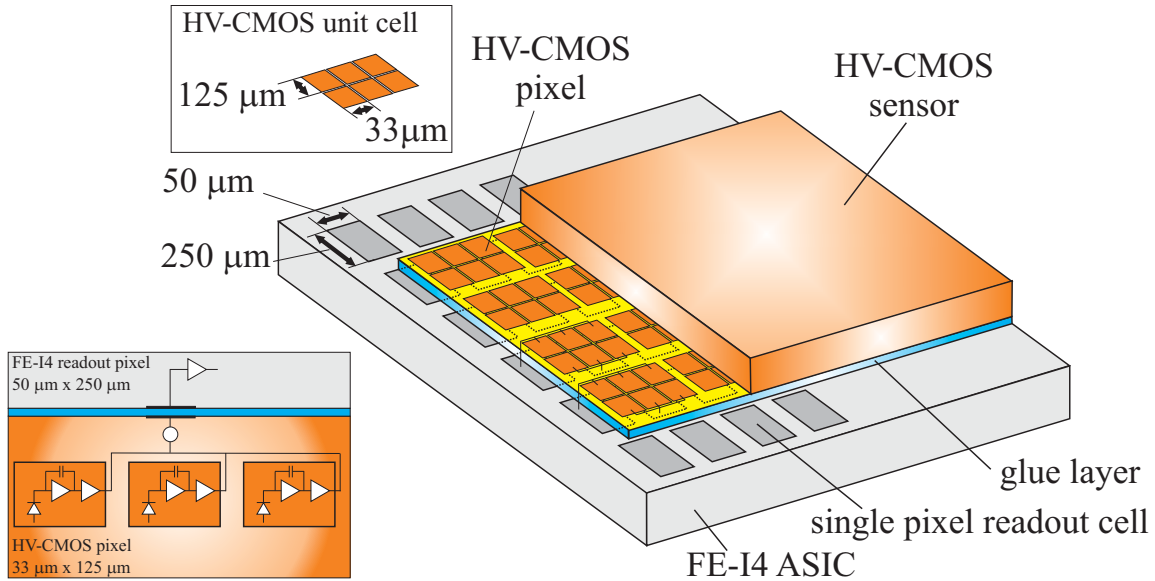


Figure 3: Schematic representation (not in scale) of the HV-CMOS to FE-I4B connections. The bottom-left inset shows how three HV-CMOS pixels (forming a so-called *macro-pixel*) are capacitively coupled to a single FE-I4B readout pixel.

tion potential for silicon at room temperature, the resulting calibration factor is  $\sim 8.6 \text{ e}^-/\text{mV}$ . The nominal operating threshold of the sensor corresponds to  $\sim 600 \text{ e}^-$ .

### 3.2 Threshold tuning

The powering, configuration and control of the AMS180v4 prototype was performed using the CaRIBOu [10] (*Control Readout Itk BOard*) test system. CaRIBOu is a modular readout system developed by the Brookhaven National Laboratory and the University of Geneva groups to characterize HV-CMOS sensor prototypes in laboratory and testbeam measurements. A Xilinx Z0706 evaluation board [8] with embedded ARM processor, based on the Zynq®-7000 All Programmable SoC, acts as main DAQ board. The system comprises various additional custom-designed and inter-connected boards (see Fig. 4):

- The CaR (*Control and Readout*) board provides powering rails, adjustable bias DACs, CMOS level translators, LVDS and clock signals, a digital injection circuitry and ADC channels. It is connected to the Xilinx Z0706 board via a FPGA Mezzanine Card (FMC) to a Very-High-Density Cable Interconnect (VHDCI) interface.
- The FE-I4 board contains the external high-voltage input for the sensor bias, the bonding pads for the FE-I4B ASIC and the required circuits for both the HV-CMOS and the FE-I4B ASIC.
- The CCPD board simply contains passive SMD components and the bonding pads for the HV-CMOS sensor. The CCPD board is attached to the FE-I4 board via a PCI Express mini-connector.

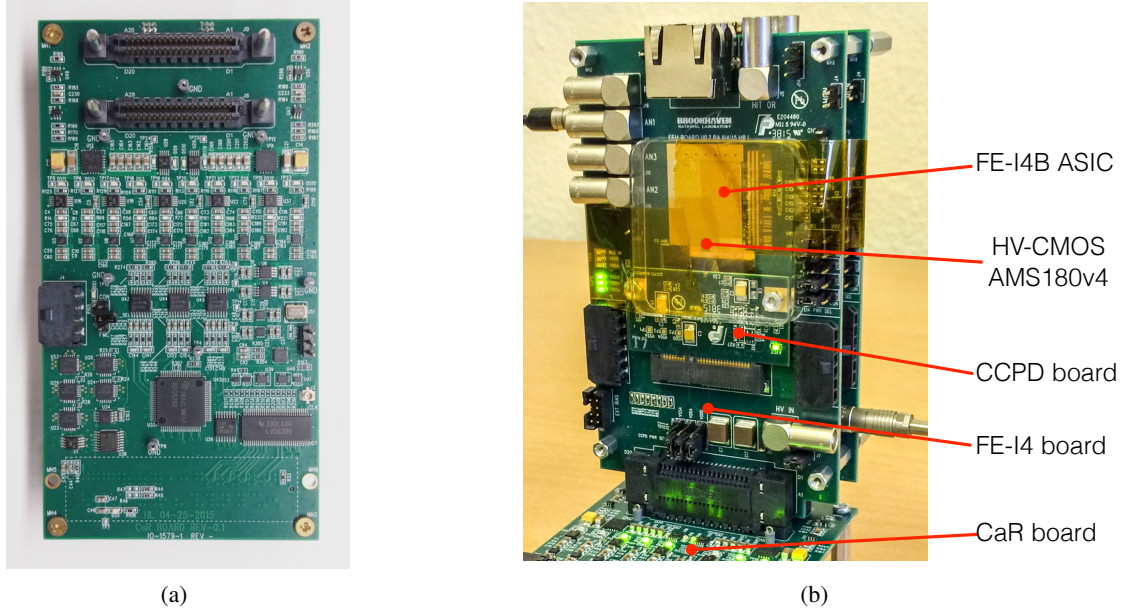


Figure 4: (a) Top-side of the CaR board. (b) The FE-I4 board with a CCPD board attached. In the configuration shown, two FE-I4 boards are connected to a single CaR board.

While the Z0706 and CaR boards were used to configure and control the HV-CMOS sensor, the glued FE-I4 chip was readout by the same RCE system as the telescope. A binary tuning procedure was implemented to minimize the threshold spread among all channels of the sensor. The tuning method consists in selecting a target threshold and then finding the optimal TDAC setting for each pixel so that the resulting threshold is close to the target within a defined tolerance. At each threshold scan, the TDAC is varied by a single unit step. A Gaussian fit to the threshold distribution obtained in the DUT after tuning resulted in a mean and sigma of  $607 e^-$  and  $73 e^-$ , respectively.

#### 4. Off-line analysis

The raw data from all six telescope planes and from the DUT are stored in ROOT [11] format for off-line processing. The software analysis framework is based on the Judith [12] program, a C++ software package originally developed for the Kartel telescope (composed of six MIMOSA-26 pixel sensors [13]). The Judith package has been adapted for the FE-I4 telescope configuration and module geometries.

The off-line analysis compares the response of the DUT to tracks reconstructed with the beam telescope. The internal alignment of the different telescope planes is performed using an iterative algorithm that minimizes the track residuals, *i.e.* the difference between the hit position measured in the plane being aligned and the predicted hit position from the track extrapolation into that plane. Noisy pixels are masked at software level before clustering. The first telescope plane is kept fixed at its nominal position as an anchor reference to define the  $X$ - and  $Y$ -axis. The track reconstruction algorithm recursively searches for clusters in consecutive planes within a limited solid angle to deal with multiple scattering. A straight line fit is then performed to the different cluster positions. The alignment algorithm corrects for the translations in the transverse plane and for the in-plane

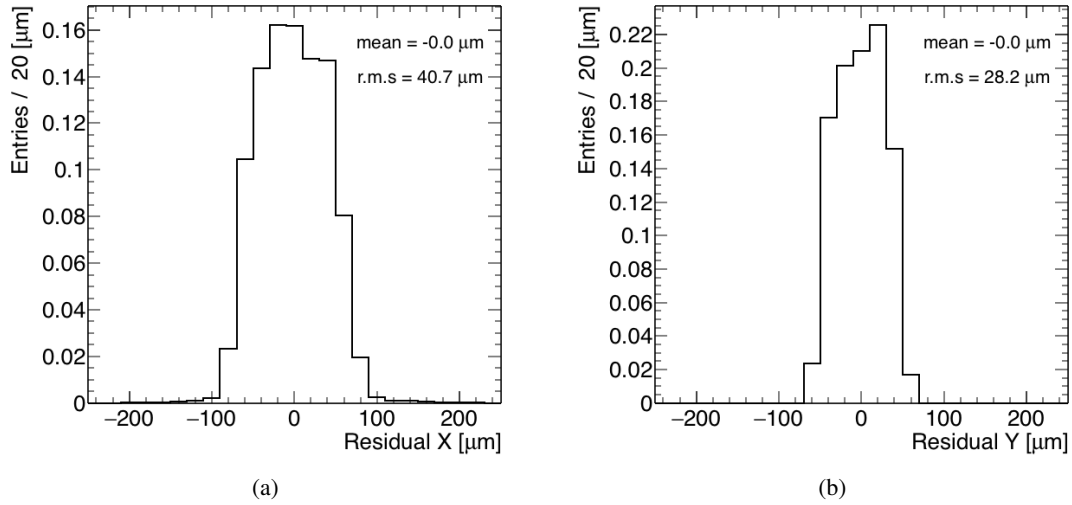


Figure 5: Normalized residual distributions of the DUT along the X (a) and Y (b) directions.

rotation around the Z-axis. Results from the telescope alignment can be found in [3]. Upper limits on the spatial resolution of the telescope were found to be  $11.7 \mu\text{m}$  and  $8.3 \mu\text{m}$  at the DUT position.

After the internal alignment of the FE-I4 telescope, reconstructed tracks are used to align the DUT. Due to the small size of the HV-CMOS sensor there was not enough sensitivity to correct for the in-plane rotation, so in this case only the two translations were considered. Single track events were selected. Tracks were required to have one hit in each of the six telescope planes, a good  $\chi^2$  from the track fit and small track gradients with respect to the beam axis. Figure 5 shows the unbiased residual distributions at the DUT after alignment along the two measuring directions. The r.m.s. of the residual distributions are in reasonable agreement with the expected intrinsic resolutions of the *macro-pixel* along the X ( $\sigma_{x,\text{exp}}$ ) and Y-directions ( $\sigma_{y,\text{exp}}$ ),  $\sigma_{x,\text{exp}} = 125 \mu\text{m} / \sqrt{12} = 36.1 \mu\text{m}$  and  $\sigma_{y,\text{exp}} = 100 \mu\text{m} / \sqrt{12} = 28.9 \mu\text{m}$ , respectively.

## 5. Results

### 5.1 Cluster size distributions

The cluster size is the number of neighbouring pixels (along both measuring directions) with a signal above threshold. It is an effective measurement of charge sharing. Figure 6 shows the cluster size distribution for the DUT at nominal operating conditions (85 V bias-voltage and  $600 e^-$  threshold). At the SPS testbeam the track incidence was almost perpendicular to the detector planes. In  $\sim 78\%$  of the events single-pixel clusters were recorded, while clusters formed by two pixels were observed in  $\sim 20\%$  of the cases. The occurrence of clusters with sizes of three or more pixels was less than  $2\%$  and thus can be safely neglected in what follows. Among the possible mechanisms leading to signal leakage into neighboring pixels (*e.g.* cross-talk between channels from capacitive coupling, diffusion of charge carriers,  $\delta$ -electrons), diffusion is the dominant one. This diffusion component is only relevant for unirradiated sensors, as it is largely suppressed by



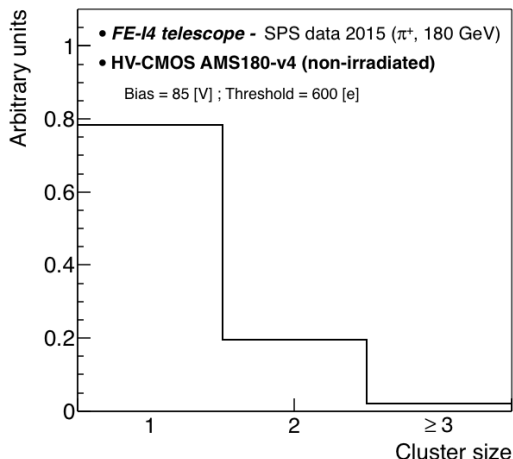


Figure 6: Cluster size distribution for normal incidence tracks and nominal operating conditions. The distribution has been normalized to unity.

charge trapping for fluences typically above  $10^{15} n_{eq}/cm^2$ , as measured on irradiated HV-CMOS prototypes with an edge-TCT technique [14] and with testbeam data [15].

Figure 7a shows the timing distribution (*i.e.* the timestamp difference of the recorded hit with respect to the trigger in units of BC, see Sec. 2.1) for all cluster sizes. The distribution shows a long tail of late (slow) hits. This tail is mainly due to a known timewalk effect in this HV-CMOS sensor design [15], so that low amplitude signals such as resulting from diffusion have a larger timing because of the slower discriminator rise time. In Figs. 7b and 7c we investigated the contribution from clusters of size one and two, respectively. In the latter case, the timing of both hits in the cluster are shown. The timing distribution of clusters of size one is very similar to that of the fastest hit of the two-pixel clusters. The slowest signals in the tail of the distribution of Fig. 7a thus correspond to the diffused charge in large multiplicity clusters (charge sharing). In order to focus on the properties of the charge collected by drift, and to limit the effects of the known timewalk present in this version of the HV-CMOS sensor, only results for the fastest hit are shown in the following.

## 5.2 Efficiency

One of the most important parameters to be studied of the AMS180v4 prototype is the tracking efficiency. For this measurement, a detector plane is considered to be efficient if the interpolated track position is located within an ellipse centered around the measured cluster with semi-axes being one and a half times the size of the *macro-pixel* (see Fig. 8). The lengths of the ellipse semi-axes correspond to five times the standard deviation of the residual distributions (see Fig. 5). The cluster position is computed as the geometrical center of the *macro-pixel*. Single track events and the track quality cuts as defined in Sec. 4 are used. The interpolated track position is required to be inside the DUT sensitive area, otherwise the event is discarded. The efficiency of a *macro-pixel* is thus simply computed as  $\varepsilon = N_{eff}/N_{tot}$ , where  $N_{eff}$  is the total number of efficient events in the pixel as just defined, and  $N_{tot}$  is the total number of selected events. Inefficient events are taken

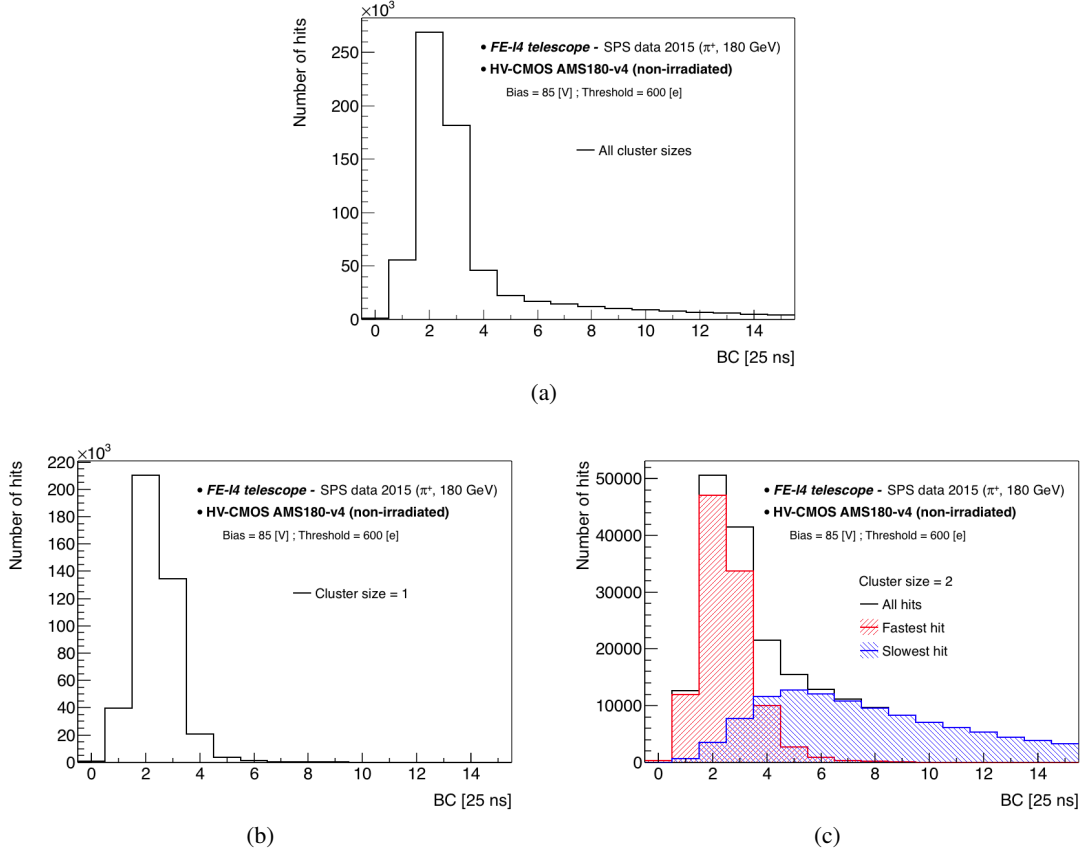


Figure 7: Timing distribution of the DUT hits in 25 ns bins for all cluster sizes (a), cluster size one (b) and cluster size two (c). In (a), all pixels are shown. In (c), the distribution of the measured time of each of the two pixels in the cluster is shown.

into account (these are events in which for a valid track interpolation at the DUT position, no hit has been measured in the DUT). Fig. 9 shows the resulting efficiency map for a bias voltage of 85 V and a threshold of 600 e<sup>-</sup>. Excluding the outermost columns and rows to avoid edge-effects due to the finite telescope resolution, an average global efficiency of  $\bar{\epsilon} = 99.7\%$  is obtained.

Thanks to the pointing resolution of the FE-I4 telescope [3] a sub-pixel resolution was achieved. Fig. 10a shows the efficiency map after merging all *S*Time pixels into a single histogram representing a *macro-pixel* ( $125 \times 100 \mu\text{m}^2$ , corresponding to three HV-CMOS pixels connected to a single FE-I4B readout channel). Figs. 10b to 10d show the relative contributions to the efficiency of different cluster sizes. The high efficiency in the central region of Fig. 10a results dominantly from events where the cluster size is exactly one ( $\sim 78\%$  of the cases, see Fig. 6). Events with a cluster size of two ( $\sim 20\%$  of the cases) contribute mainly to the edge regions, as expected from charge sharing between neighbouring pixels. The less common events in which the cluster contains three or more pixels are localized at the four corner regions.

The efficiency as a function of the discriminator threshold is shown in Fig. 11 for a bias voltage of 80 V. As expected, the efficiency drops in the low-threshold (noise dominated) and high-threshold (low signal) regions. The region for which the efficiency is higher than 99.5% is between

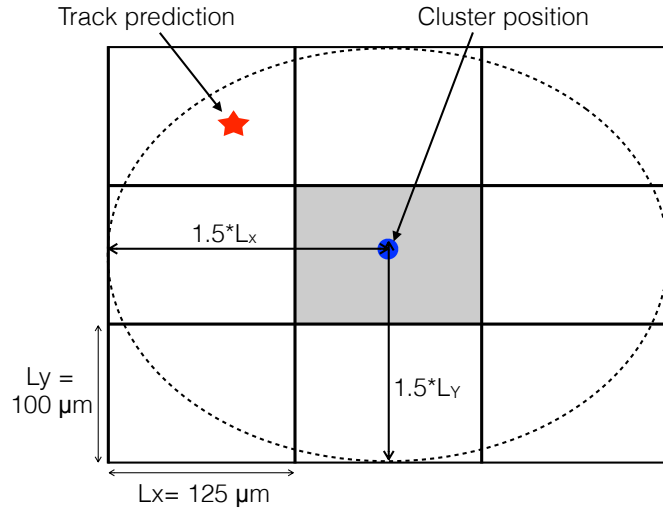


Figure 8: Definition of the area used to calculate the efficiency. Each  $125\ \mu\text{m} \times 100\ \mu\text{m}$  *macro-pixel* (gray area) is formed by three single HV-CMOS  $125\ \mu\text{m} \times 33\ \mu\text{m}$  pixels.

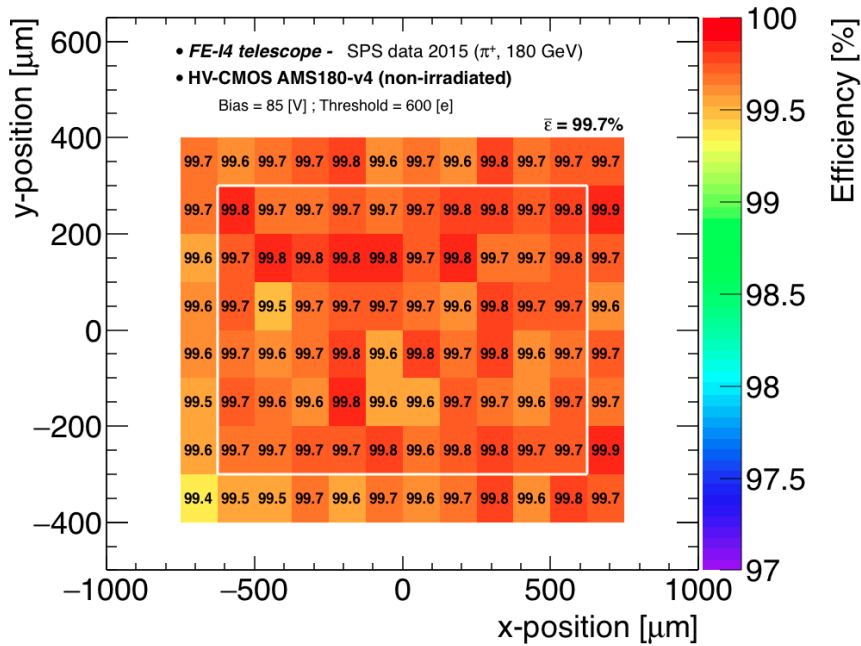


Figure 9: Efficiency map of the AMS180v4 sensor. For the computation of the average global efficiency,  $\bar{\epsilon} = 99.7\%$ , the pixels inside the white box are used.

385 and  $690\ e^-$ .

The efficiency as a function of the sensor bias voltage is shown in Fig. 12a for a threshold of  $600\ e^-$ . The large statistical uncertainty of the first data point (10 V bias voltage) is due to the fact that, accidentally for this particular run, the ROI region was not set. Fig. 12b shows the in-pixel efficiency for a bias of 20 V (to be compared with Fig. 10a where the bias voltage was 85 V at the

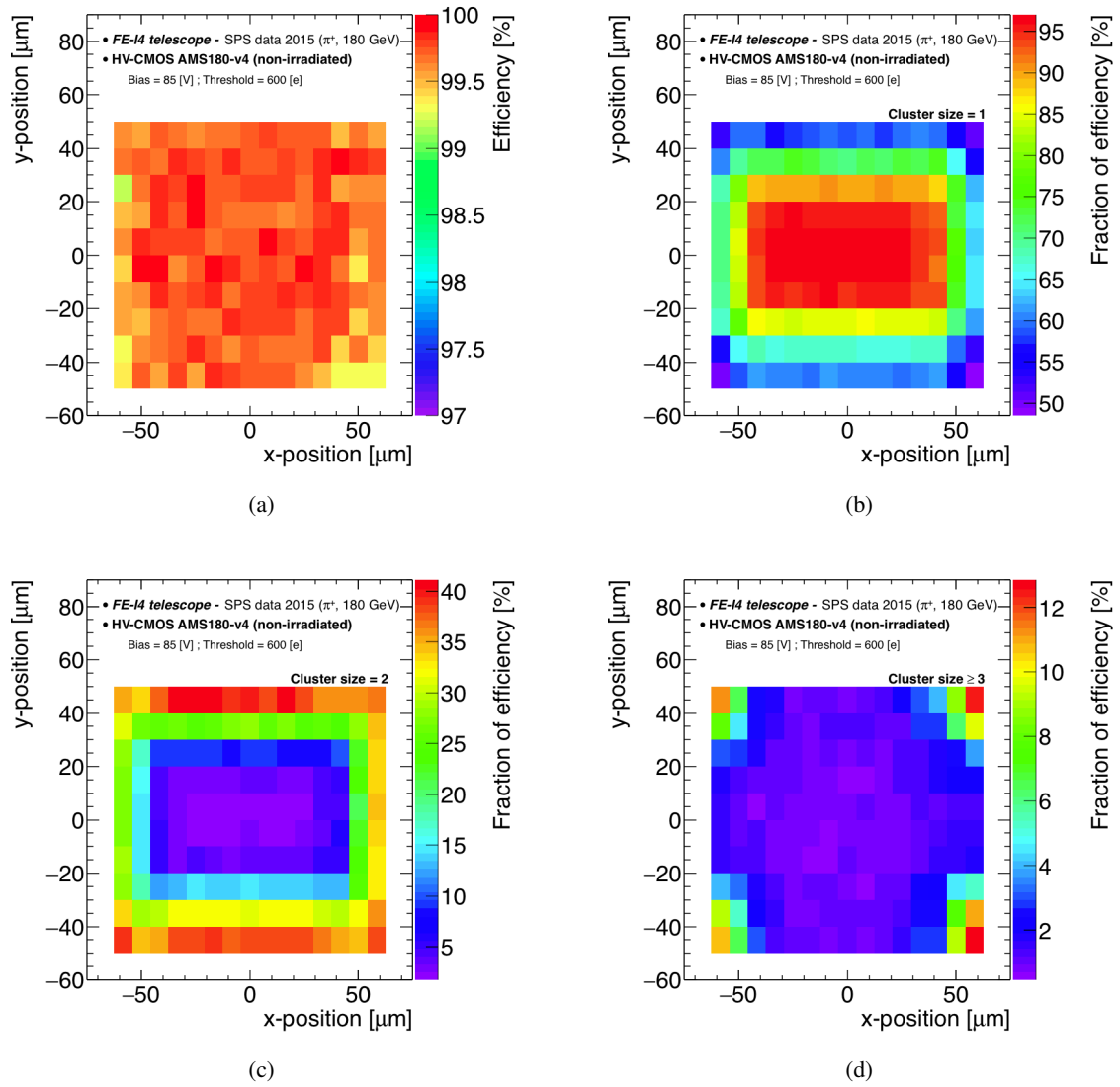


Figure 10: (a) Efficiency inside a *macro-pixel* of  $125 \mu\text{m} \times 100 \mu\text{m}$ , corresponding to three single HV-CMOS pixels connected to a FE-I4B readout cell. (b-d) Relative contributions to the distribution shown in (a) from pixel clusters of different sizes.

same threshold). The lower depletion region is source of inefficiencies at the pixel edges. Overall, the relatively high efficiency at lowest bias voltages indicates that, in addition to drift, part of the charge is collected by diffusion.

The efficiency has been evaluated in each of the sixteen 25 ns time intervals used for the readout of the DUT. Figure 13a shows the efficiency per time-bin for different bias voltages for the fastest hit in the cluster. The shape of the distributions are similar to that already shown in Fig. 7b. Due to some existing delays (*e.g.* different cable lengths, clock-jitter) between the trigger and the DUT readout, it is assumed that the time-bin for which the maximum is reached corresponds to that of the passage of the incident particle. Most particles are detected in a two-bin interval. For increasing bias voltages the depletion region enlarges and the maximum efficiency increases.

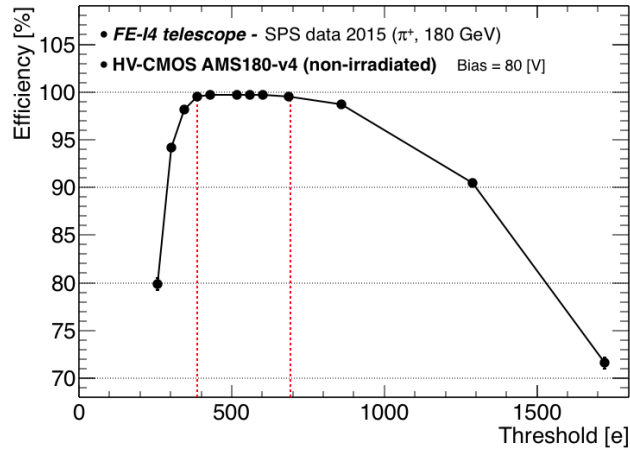


Figure 11: Efficiency as a function of threshold. The two vertical dashed-lines indicate the operating region for which the DUT efficiency is larger than 99.5%.

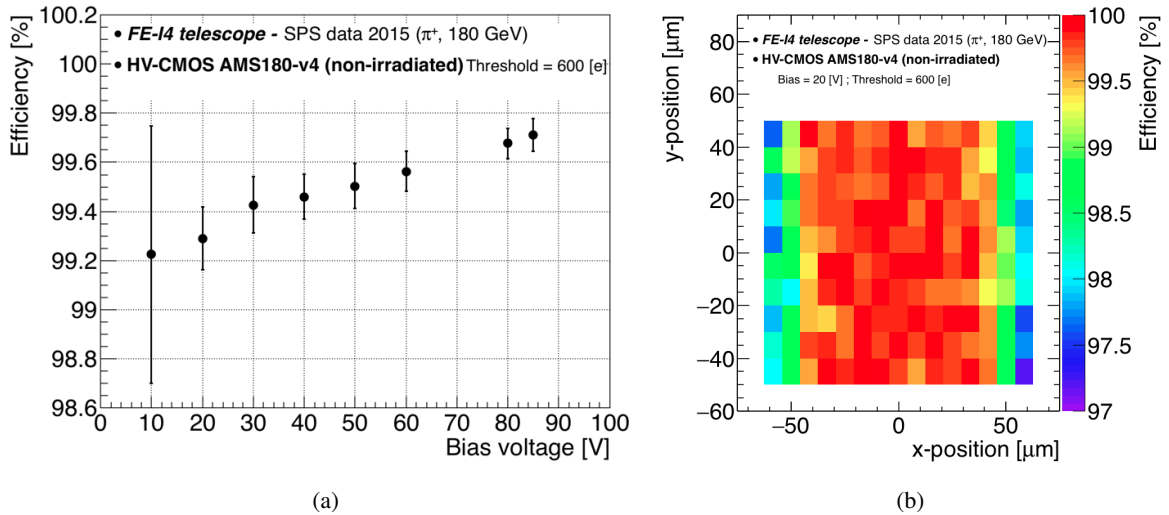


Figure 12: (a) Efficiency as a function of bias voltage. (b) In-pixel efficiency for 20 V bias voltage. The reduced efficiency on the vertical edges is due to a higher charge sharing as from the finer pixel granularity along the vertical direction (the *macro-pixel* shown corresponds to three  $125 \mu\text{m} \times 33 \mu\text{m}$  pixels).

Fig. 13b shows the cumulative efficiency as a function of 25 ns time-bins. The distribution has been computed with respect to the consecutive maxima in Fig. 13a. At 85 V bias voltage, an efficiency higher than 90% is achieved after three BCs.

Figure 14 demonstrates the effect of the threshold on the timing distribution of the DUT. As the threshold is lowered, it can be observed that the dispersion of the time of arrival of the hits is reduced. This is further evidence of the large variation of the rise time of the signal. In the case where the rise time of the signal would be the same for small and large signal, a reduction of thresh-

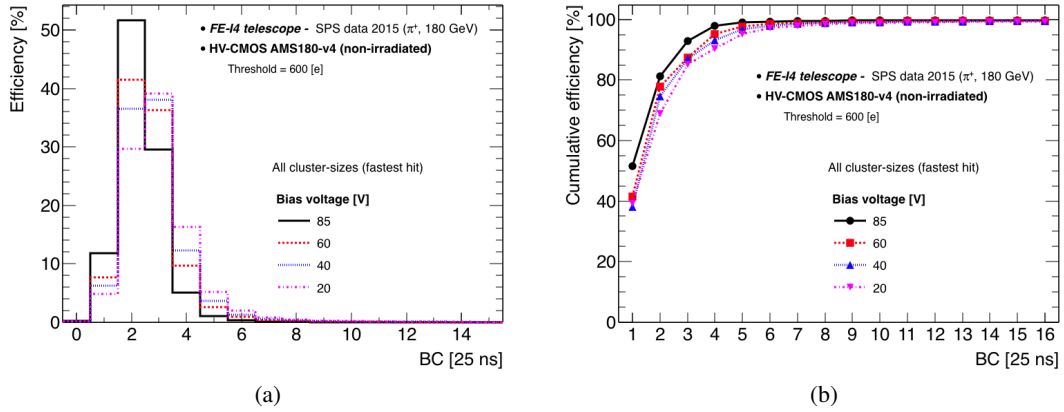


Figure 13: (a) Efficiency and (b) cumulative efficiency in bins of 25 ns for different sensor bias voltages. For cluster sizes of two or more, only the fastest hit is shown. The first data point shown in (b) corresponds to the maxima of the distributions shown in (a).

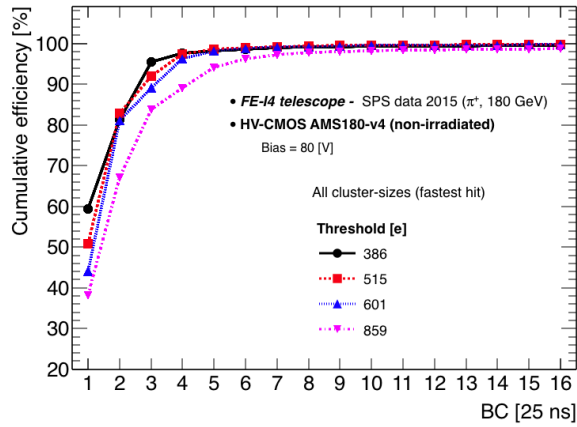


Figure 14: Cumulative efficiency in bins of 25 ns for different thresholds. For cluster sizes of two or more, only the fastest hit is shown.

old would only yield an increase in efficiency. However it is observed here that the improvement of the timing distribution spread is occurring even when the threshold is reduced within the plateau of efficiency featured in Fig. 11.

## 6. Conclusions

A HV-CMOS sensor prototype produced in the AMS 180 nm technology has been tested in November 2015 at the H8 beamline of the CERN SPS. A FE-I4B ASIC has been glued to the HV-CMOS sensor to read the signals via capacitive coupling. For the first time, the CaRIBOu system has been used to power, configure and control the AMS180v4 chip. A threshold uniformization using a binary tuning algorithm yielded a final threshold dispersion of  $\sim 70 e^-$  about a mean of  $\sim 610 e^-$ . The FE-I4 beam telescope has been used to reconstruct the tracks to evaluate the performance of the

HV-CMOS prototype. An average global efficiency of 99.7% has been measured for a bias voltage of 85 V and an operating threshold of 600 e<sup>-</sup>. It has been measured that the sensor can be operated with an efficiency higher than 99.5% within a threshold range between ~400 and ~700 e<sup>-</sup>. The timing performance of this prototype is not yet sufficient to be operated in a HL-LHC experiment as an efficiency higher than 90% is measured within a three 25 ns BC window. New versions of the AMS chip have already been produced in both 350 and 180 nm technologies to improve the time response of the sensor.

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