Smart Equipment Technology

Flip Chip Die Bonding: An Enabling Technology for 3DIC Integration

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3-Dimensional Integration of Integrated Circuits is a method to build greater functionality into ever-smaller spaces for electronic circuitry, wherein dice of varying sizes, materials, or even application types are electrically and mechanically bonded together. As chip sizes increase and packaging bump sizes decrease, a wide variety of new problems has arisen in the areas of bonding materials, methodologies and equipment.

This paper will explore some of these new challenges, highlighting the inherent advantages and challenges of various options. Specifically, the methodologies of chip-to-chip, chip-to-wafer, and wafer-to-wafer bonding will be examined, followed by discussions of some material choices and the associated bonding techniques such in-situ reflow or thermo-compression. Depending on the interconnect density and the selected bonding technology, either pick-and-place or high accuracy die bonders can be employed for attachment of the dice to the substrate, each with its own tradeoffs. Finally, a method of first placing the chips with high accuracy, followed by collective bonding will be explored for a customer application, including electrical and alignment test data.

Each scenario places special requirements on the bonding tool, so incremental modifications and enhancements to the flip chip bonding platform will be outlined and explored to gauge their impact in enabling 3DIC integration. In particular, hardware and materials to reduce oxides on the bonding surfaces, as well as point-of-use die testing before bonding will be highlighted.