## Chip to wafer direct bonding technologies for high density 3D integration

L. Sanchez<sup>(1)</sup>, L. Bally<sup>(1)</sup>, B. Montmayeul<sup>(1)</sup>, F. Fournel<sup>(1)</sup>, J. Dafonseca<sup>(1)</sup>, E. Augendre<sup>(1)</sup>, L. Di Cioccio<sup>(1)</sup>, V. Carron<sup>(1)</sup>,

CEA, Leti, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble, Cedex 9, France (1)

STMicroelectronics, 850 Rue Jean Monnet, 38926 Crolles Cedex, France (2)

SET, 131 imp. Barteudet, 74490 St Jeoire, France (3)

### Abstract

We demonstrate chip to wafer assembly based on aligned Cu-Cu direct bonding. A collective die surface preparation for direct bonding has implemented to develop dies direct bonding, defect free. An accurate pick and place equipment was adapted to ensure a particle free environment. After a damascene-like surface preparation, chips were bonded with less than 1 $\mu$ m misalignment. 400°C bonded daisy chains on die to wafer structure are perfectly ohmic. Concurrently, to overcome speed limitation of pick and place technique, a self assembly technique chip is developed. This technique is based on capillary effect for self alignment and direct bonding for assembly. A less than 1  $\mu$ m alignment accuracy and a 90 per cent self assembly process yield are obtained.

### Introduction:

Chip-to-Wafer technologies are promising solutions for high density 3D integration application to overcome the limitation of Wafer-to-Wafer in term of staking yield, alignment accuracy and reproducibility along the wafers. Direct Cu bonding was developed at Leti to enable in situ Chip/Wafer electrical interconnection at ambient air and low temperature and it is one of the most promising approaches for 3D integrated circuits [1]. This process has reached a maturity and a promising reliability for wafer-to-wafer and chip-towafer stacking [2-3-4]. We present here the recent advances in chip to wafer structures made by a combination of direct Cu bonding and high alignment accuracy pick and place process. For the first time a collective dice treatment for direct bonding is presented. Furthermore, the first electrical test on a high density daisy chain made by chip-to-wafer technologies is reported on this paper. Nevertheless accurate pick and place technologies remain speed limited. To overcome speed limitation of accurate pick and place different techniques have been proposed. The self-alignment by capillary effect is the most advanced one [5-6-7]. In the last part recent results on self-assembly based on capillary effect and direct bonding are reported.

## Die collective treatment and pick and place developments for direct bonding

For direct bonding technologies, extremely low surface contamination is required to ensure the perfect quality of the bonding interfaces. It is the most critical point for dice direct bonding because dicing and dice handling steps could generate high particles contamination. To optimize die surface cleaning, we have developed a dice holder compatible with industrial 200 mm / 300 mm microelectronic cleaning tools (Fig 1).



Fig.1: Dice holder

For this study, one centimeter square silicon chips are bonded on 200 mm silicon wafer. A thermal 200 nanometers silicon dioxide layer is grown on die chip and wafer. Dice and wafer surfaces were subjected to a combination of treatments to remove particles and to enhance the surface hydrophilicity. Automatic particles counting by optical microscope observations show that more than 90% of particles are removed by the collective cleaning for particle size higher than  $5\mu$ m (Fig.2).



Fig. 2: particles removal efficiency for particle size higher than  $5\mu$ m.

T. Signamarcheix<sup>(1)</sup>, R. Taibi<sup>(2)</sup>, S. Mermoz<sup>(2)</sup>, G. Lecarpentier<sup>(3)</sup>

The removal of particles of less than 5µm is evaluated by Scanning Acoustic Microscopy (SAM) observation of the bonding interface. For this technic of characterization, the radius of the smallest detectable unbonded area is about 50-100  $\mu$ m. Such defect radius matches with a particle size 10<sup>3</sup> or  $10^4$  times smaller [8]. Furthermore, in the case of a thermal silicon-dioxide direct bonding, the bonding defectivity at room temperature could be explained only by particles contamination [8]. Fig. 3 is a SAM observation of the structure obtained for a collective bonding at room temperature just after the collective dies cleaning. Here, the host wafer is directly reported on chips loaded on the holder. The collective direct bonding is induced by the using of a low strength uniformly distributed on the host wafer. Black areas match with bonded areas. 100% of dies are bonded and 80% of dies are bonded without bonding defects. This SAM observation demonstrates the excellent bonding quality of the chip to wafer interface and confirm the high efficiency of the collective cleaning. Compared with the manual process (dies are handmade cleaned and bonded one by one), the collective process allows to significantly decrease bonding defects at the chip to wafer bonding interface (Fig.3).



Fig.3: SAM observation of a bonded structure after collective cleaning and bonding and after handmade cleaning and bonding.

To limit particles contamination during processing, specific developments were realized on an SET – FC300 pick and place equipment. A local microenvironment was created into the equipment to protect the wafer surface during the chip's bonding (Fig 4).



Fig. 4: illustration of the microenvironment realized by the SET Company on the FC300 equipment to limit the particulate contamination on the wafer during the chip-to-wafer bonding.

The efficiency of the FC300 microenvironment is evaluated by automatic surface inspection on a wafer. A wafer was placed on the equipment during one hour (the mean time to place 60 dies on a wafer) firstly without robotic movement then with robotic movements (arm, optic module and chuck movements). For each case, the particles contamination remains relatively low and it should not introduce additional defectivity on chips bonding interfaces (Fig 5).



Fig. 5: Automatic surface inspection on a 200 mm silicon wafer after a wait of 1h on the FC300 equipment without/with robotic movements.

In this first part, we demonstrate that we control particles contamination for nearly all steps of chips bonding process. Anyway dies are loaded manually in the FC300 bare dies tray and this can explain the remaining defectivity. This loading will have to be improved to optimize control of particles contamination.

# Experimental structures for direct copper bonding and electrical results

After trench opening in deposited silicon dioxide, TiN and Cu seed layers were deposited. Cu filling was carried out by electroplating and then annealed at 400°C. Optimized damascene like process was used to obtain a smooth surface and to adapt the topology between the silicon oxide and copper areas. Dies surfaces were then subjected to a collective combination of treatments to clean surfaces and enhance the hydrophilicity. Fig 6 is an infrared observation of the structure obtained for an aligned chips-to-wafer at room temperature.



Fig. 6: infrared observation of 17 dies assembled by aligned direct copper bonding in FC300 equipment.

Dark areas or areas with interference patterns match with unbonded areas. The bonding defectivity remains high and could be due to the handmade bare dies tray loading. This loading must be improved to ensure a free bonding defect.

Chip-to-wafer bonding was performed using the alignment capability of the FC300 equipment and two sets of alignment patterns defined on chip and host wafer surfaces. The alignment accuracy was measured after bonding by reading vernier patterns through the chip and the wafer with an infra red microscope. Fig. 7 shows that the measured misalignment remains lower than  $1\mu m$  in both x and y axis on left and right alignment verniers.



Fig 7: chip-to-wafer misalignment in both x and y directions measured on the left and right alignment patterns of 50 chips. Vernier scale resolution is 200 nm.

The electrical interconnect by aligned bonding process was validated by measuring the I-V characteristic of a high density bonded daisy chain (~ $1.5*10^6$ /cm<sup>2</sup>). Description of the daisy chain is presented in figure 8.



Fig 8: SEM observation of the daisy chain and layout description.

The behavior of a 400°C bonded daisy chain on die to wafer structure is perfectly ohmic and comparable in resistance with wafer to wafer structure (Fig 9). Furthermore Chip-to-Wafer Cu interconnects made by this approach have a very tightly distributed resistivity.



Fig 9: I-U characteristics of the daisy chain measured on 8 dies.

Dice bonded on wafers allow the measurement of the electric resistance of the bonded copper lines from room temperature to 400°C. Fig. 10 is the description of the tested structure.



Fig 10: description of the tested structure layout used to study annealing effect on structure resistivity.

There is an electrical resistance measurable for the room temperature bonded structure meaning that the bonding is effective at room temperature (Fig. 11). This resistance is quite high, 9.5 ohms and it could be explained by the presence of an oxide or a bonding interface partially sealed. With temperature, the resistance decrease and the resistance reaches its lowest value at 300°C (3.5 ohms). This lowest value matches perfectly with the theoretical resistance of the interconnect calculated with theoretical resistivity of copper.



Fig 11: electrical behavior of a 640 x  $3\mu m^2$  copper bonded lines with temperature.

#### Chip Self assembly

Conventional chip-to-wafer assemblies by pick and place equipment can't allow both high alignment accuracy and high assembly throughput. In order to allow both high throughput and high alignment precision, Leti has developed a promising dies self-assembly technics. Our technique is the addition of two effects. Firstly a capillary effect for self alignment and secondly after water evaporation a direct bonding for assembly. Small water drops were used to align dies to wafer substrate. Structures realignment results from water surface tension minimization between two fluid restricted areas (fig. 12).



Fig. 12: Self-alignment assisted by capillary effect and direct bonding.

To avoid water overflowing, a high fluid containment is required. Fluid restricted areas are made by physical and/or chemical contrast. The physical contrast is based on canthotaxis effect [6]. 8x8mm silicon pads with 50nm silicon oxide on the top surface create physical discontinuities on the chip surface. Pads height is  $20\mu$ m. The chemical contrast is achieved by the creation of hydrophilic (water drop contact angle  $<5^{\circ}$ ) and hydrophobic areas (water drop contact angle  $\sim95-110^{\circ}$ ). Different configurations are implemented to correlate the fluid containment quality and alignment accuracy. Three type of water layer containment have been evaluated: fully hydrophilic pad, fully hydrophobic pad and mixed structures. Mixed structures are formed by a hydrophilic pad top layer surrounded by hydrophobic edges (fig.13).



Fig.13: The three different types of fluid containment.

For each configuration, fig. 14 shows the bonding yield and the alignment yield ( $<1\mu$ m) for 15 dies assemblies. The upper chip is released a few millimeters above the liquid drop.



Fig 14: Sub-micron alignment (X-Y axis) and bonding yield in self-assembly process with different sort of containment.

Hydrophilic and hydrophobic structures present an exact opposite behavior. Hydrophobic structures present high containment capabilities due to the hydrophobic edges, but inhibit direct bonding process. Mixed structures seem to allow both high submicron alignment yield and high direct bonding yield. Furthermore, the exactly same behavior is observed for pad height of  $8.5\mu$ m and  $80\mu$ m.

The perfect water layer containment during self-alignment could be observed by infra-red high speed observations (Fig. 15) and accurate alignment measurements are performed with verniers patterns by microscope infra-red measurement (Fig. 16). Alignment accuracy measured is lower than  $1\mu m$  in both X and Y axis.



Fig.15: perfect water layer containment by hydrophobic pads observed by high speed Infra Red camera.



Fig.16: Perfect vernier patterns superposition observed with Infra-red microscope.

The fig. 17 is a SAM observation of self-aligned structure after annealing at 200°C during 2 hours. Self-assembled structures present perfect bonding interfaces without defects.



Fig 17: SAM observation of a self-assembled structure after annealing at 200°C during 2 hours.

### Conclusions

We have developed a die surface treatment compatible with most 200 / 300 mm microelectronic equipment. It allows to reach very low defectivity at dice's bonding interfaces. Furthermore, with this collective treatment, dice bonding technologies could be manufactured at industrial scale. With optimized FC300 equipment for direct bonding, we demonstrate chip-to-wafer stack realized by combination of direct copper bonding and high alignment accuracy pick and place process. A die misalignment less than 1µm could be reached. The loading of chips on the FC300's bare dies tray have to be improved to control perfectly the particle contamination. Nevertheless, copper interconnections by direct bonding were validated on a high density daisy chain and present a perfectly ohmic behavior. The impact of the direct bonding interface on measured resistance seems to become negligible after a 300°C annealing. Concurrently, to overcome speed limitation of accurate pick and place equipment, a chip self-assembly technique based on capillary effect and direct bonding is developed. Mixed structures based on topological and chemical water containment allow both high submicron alignment yield and high direct bonding yield. By its assembly flexibilities, high density interconnection compatibility and no underfill need, chip to wafer direct bonding with alignment could become a key technology for 3D integrated devices.

### Acknowledgments

Parts of this work has been performed in the frame of the PROCEED project founded by the French authorities (at both regional and ministerial levels) and by European authorities (FEDER).

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