High Accuracy Placement, In-situ Reflow or Thermo-Compression Bonding Enabling High Density and Fine Pitch in 3D-IC with Chip to Wafer Bonding Approach

Illustrated by an Application using Micro-Insertion

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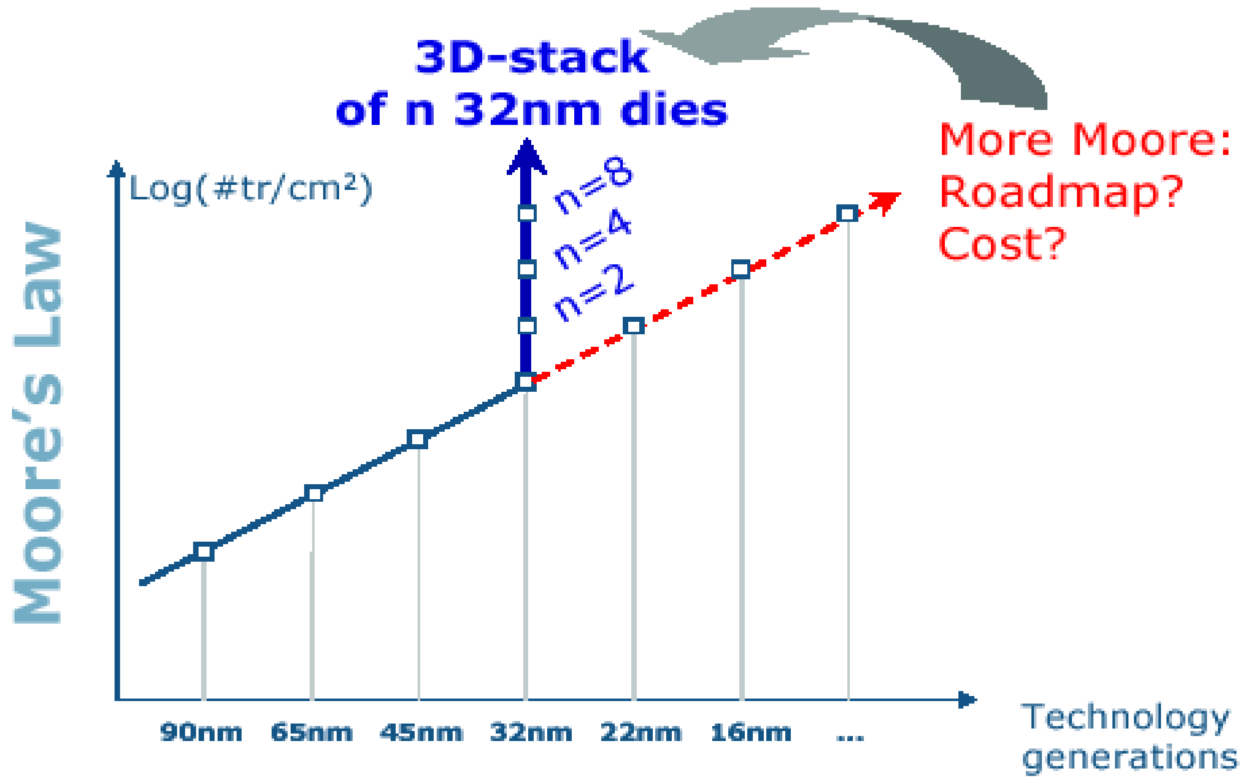
OUTLINE

- Introduction
- Wafer Stacking Vs Chip-to-Wafer Bonding
- Chip Bond Processes
- Benefit of the Self Leveling Function
- Conclusion

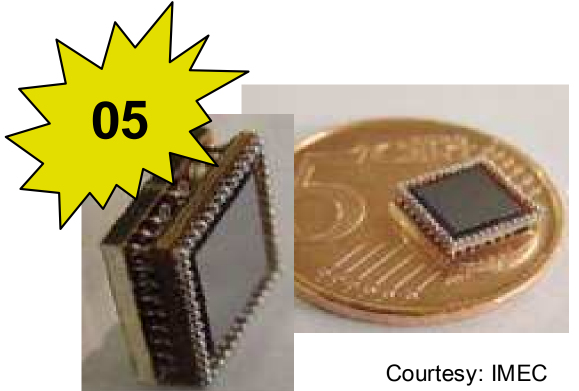
WHY 3D

- 3D provides an alternative to scaling

- Drivers are:
  - Performances
  - Form Factor
  - Cost



3D, NOVEL TECHNIQUE ?



Courtesy: IMEC

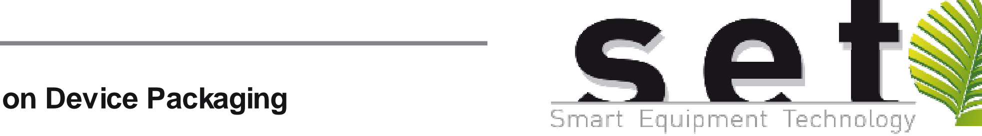
- **MEMS RF Device: assembled to a Logic with Package on Package Approach**
  IMEC

Courtesy: LETI photos: ARTECHNIQUE

- **Memory stack: Flip Chip on Silicon Interposers, stacked together with TSV**
  LETI

Source: Samsung

- **Memory stack with TSV**
  SAMSUNG



PLACEMENT SCHEMES

- **3D Assembly by Chip or Wafer Stacking enables developing Very High Density, Multifunction Devices and satisfies the demand for Higher Packaging Miniaturization**

- **Available 3D-Assemby Technologies**
  - Chip-to-Chip (C2C/D2D)
  - Chip-to-Wafer Bonding (C2W/D2W)
  - Wafer-to-Wafer Bonding (W2W)

PLACEMENT SCHEMES

3D Advanced Packaging

	SiP branch	3D branch		
Objectives	Integration of heterogeneous chips of different sizes (memories + µP + MEMS + imagers ....)	Stacking of homogeneous chips, mainly memories: *Samsung, NEDO, Tezzaron*		
Definition	SiP	3D ICs		3D stacking
Stacking type	Die to substrate	Wafer stacking	Die stacking	Die stacking
C2W vs. W2W		W2W	C2W or C2C	C2C
Interconnect type	Wire bonding (no TSVs needed) or Flip Chip	TSVs		Wire bonding
		OR		
		TSVs at chip's edges	TSVs "everywhere"	
Laser vs. DRIE		Laser or DRIE	DRIE rather than laser	
FE vs. BE	Back-end of line	Back-end of line if laser is used	Front-end of line if DRIE is used	Back-end of line

S
E
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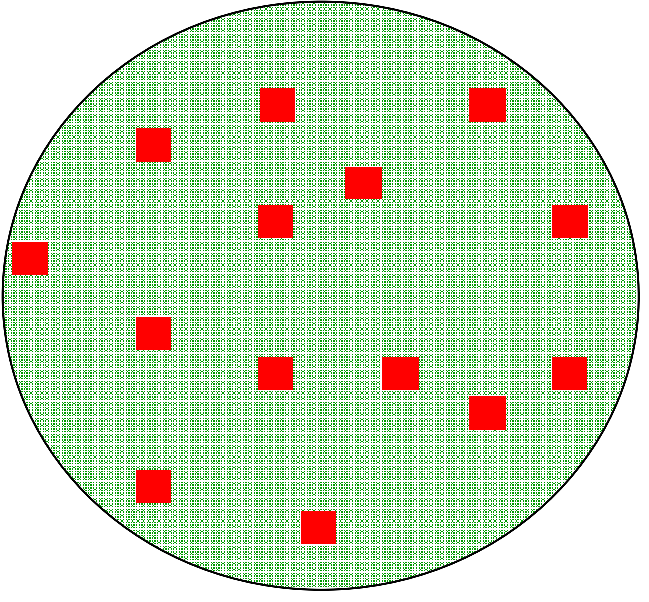
CHIP TO WAFER Vs. WAFER STACKING

- **WAFER STACKING**
  - ☺ High Throughput
    → Wafer Level
  - ☹ Component size must be identical
  - ☹ Yield ?



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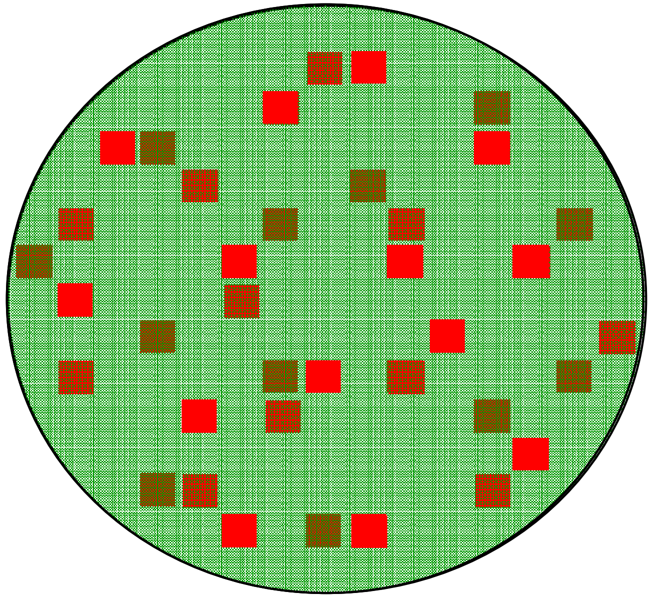

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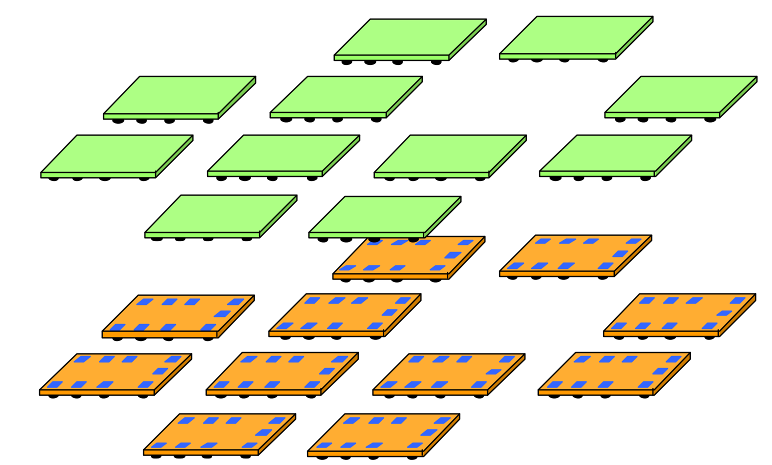

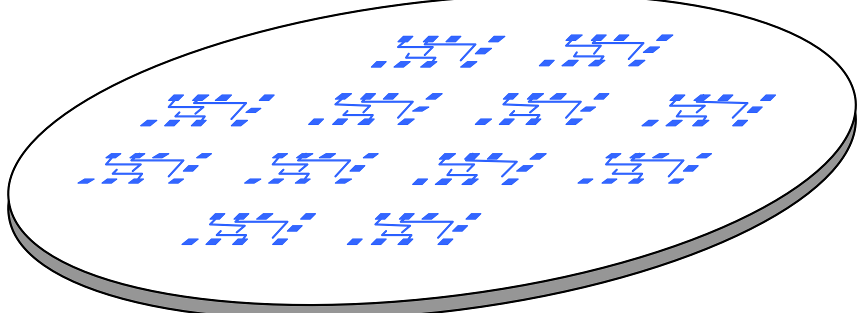

- **CHIP-TO-WAFER**
  - ☹ Lower Throughput
    - → Single Chip Placement
  - ☺ High Yield
    - → Known Good Die
  - ☺ Flexibility
    - → Component size
    - → Different Technologies

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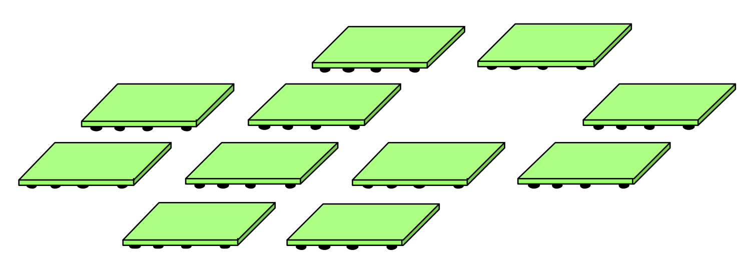

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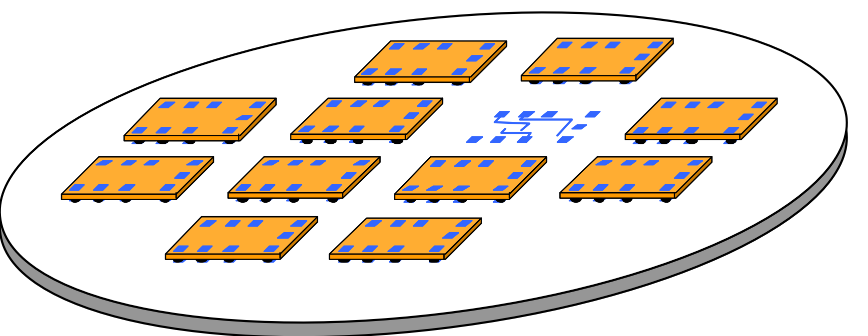

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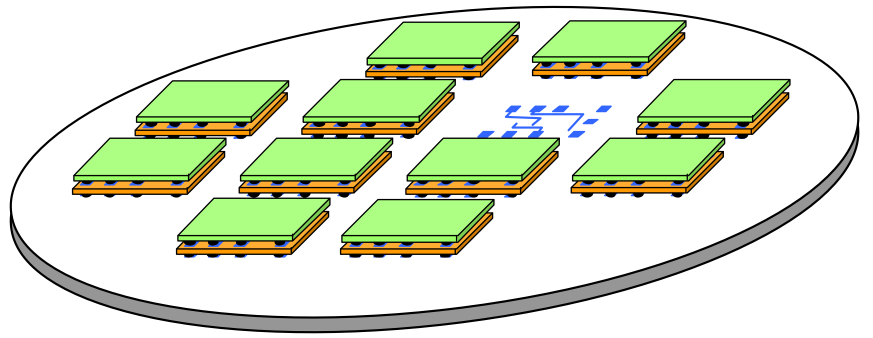

3D-IC, TECHNOLOGIES AND EQUIPMENT

3D IC technologies and equipments

	Via drilling	Via filling	Wafer/Chip bonding: C2W	Wafer/Chip bonding: W2W	Thinning
Technologies	Laser drilling DRIE Photolithography	Electroplating CVD Photolithography	Adhesive, fusion oxide or metal-metal bonding Chip alignment	Adhesive, fusion oxide or metal-metal bonding Wafer alignment	Grinding (BG) CMP Wet etching Plasma etching
Equipments	Laser OR DRIE equipment Coater Mask aligner OR stepper	Metal deposition system Coater Mask aligner OR stepper	Flip Chip Bonder	Wafer bonder Wafer aligner	Thinning equipments Temporary bonding equipments

5 chip stack

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S E T

CHIP BONDING PROCESSES (FC)

Thermo compression

- Temperature, Force / Gap control
  - Bumps Au, In, Cu…
  - Bumps Au, Ni/Au with Adhesive
    - NCA
    - ACA
    - ICA

Reflow

- Temperature / Gap control
  - PbSn, SnAg, 80AuSn, In Bumps
- Temperature / Fluxing
  - PbSn, SnAg, In Bumps (+ flux)

direct

- Low Force
  - No intermediate layer

——— Device Bonder   – – – – – Pick and Place

ACCURACY REQUIREMENT FOR D2W BONDING

3D DIE INTERCONNECT
Two Distinct Applications and Technologies

Applications	Memory Die	Logic
I/O Per Die	< 100	> 5,000
Justification	Miniaturization	Increased electrical performance
I/O Pitch	> 300µm	< 25µm
Minimum Via Size	> 50µm	< 5µm
Device Configuration	Stacked (Flash, DRAM, SRAM)	Processor and cache, ASIC, and cache Logic with Analog, MEMS, 3-5 Semiconductor
Interconnect Cost	< $0.30/die	> $3.00/die
Vertical Interconnect Technology	*Packaging-like:* Aqueous plating Molding/lamination Laser drill	*Fab-like:* Vacuum deposition Spin coating RIE

BENCHMARKING DIFFERENT 3D APPROACHES

Placement Accuracy for 3D-IC >> 1 ~ 3 µm

	3D-SiP	3D-WLP			3D-IC
		UTCS	VIA-1	VIA-2	
3D Interconnect Technology	Package Interposer	Embedded Thin Die	Conformal Cu TSV	Cu-Filled TSV	Cu-nail TSV
Interconnect density	'package-to-package'	'around' die	Through Si	Through Si	Through Si
Peripheral	2-3 / mm	10-50 / mm	6-20/mm	25-50/mm	>100/mm
Area-Array	4-11 / mm²	100-2.5k/mm²	44-400/mm²	625-2.5k/mm²	> 10k/mm²
3D-TSV pitch	-	-	50-150µm	20-40µm	<10µm
3D-interconnect pitch	300-500µm	20-100µm	-	-	-
3D-TSV diameter			40-100µm	15-25µm	1-5µm
Die Thickness	50µm	10-20µm	50-100µm	25-50µm	10-20µm

Source: IMEC

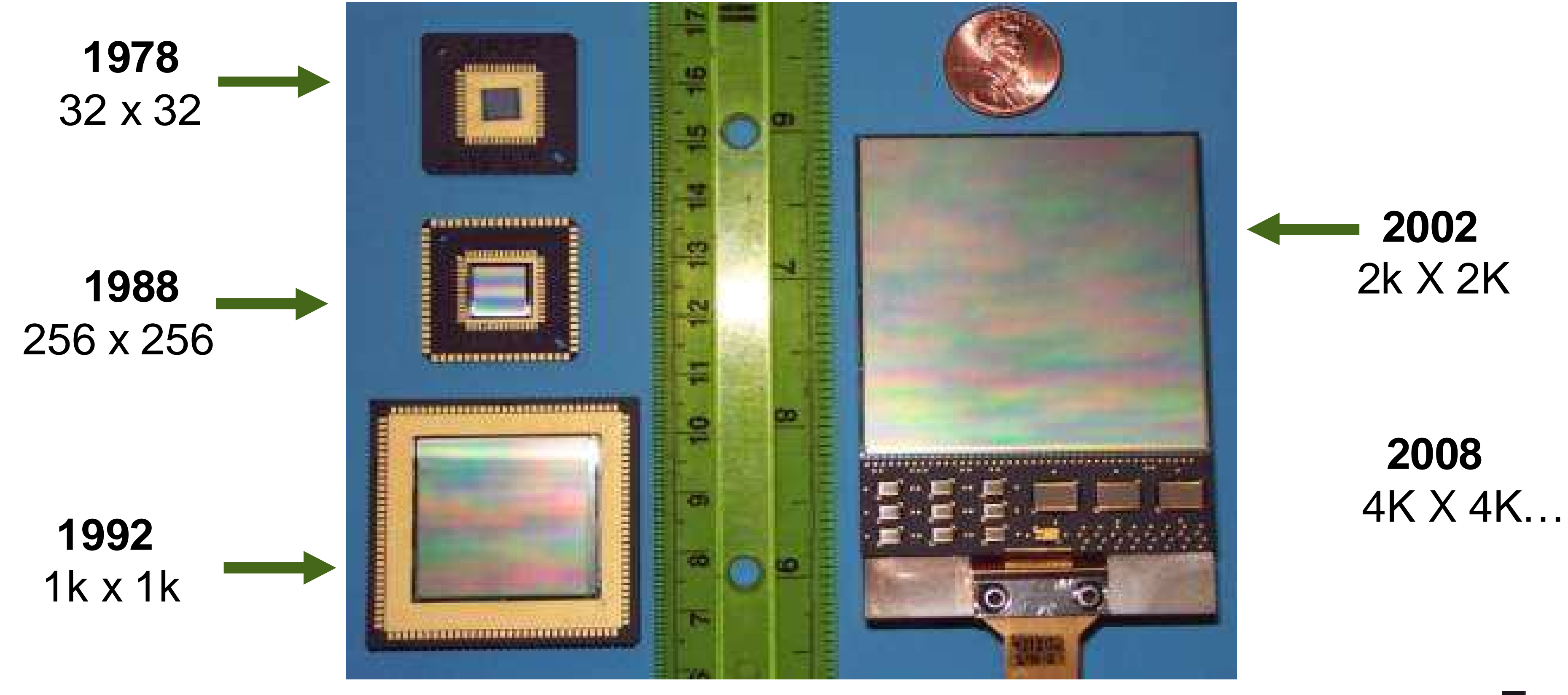
CHIP TO CHIP, HIGH ACCURACY, HETEROGENEOUS INTEGRATION IS THERE FOR DECADES

- **Infrared Focal Plane Arrays with Bonding of High Density, Fine Pitch, HgCdTe or GaAs Die to Silicon CMOS Read Out IC is achieved successfully for over 30 years**

1978
32 x 32

1988
256 x 256

1992
1k x 1k



2002
2k X 2K

2008
4K X 4K…

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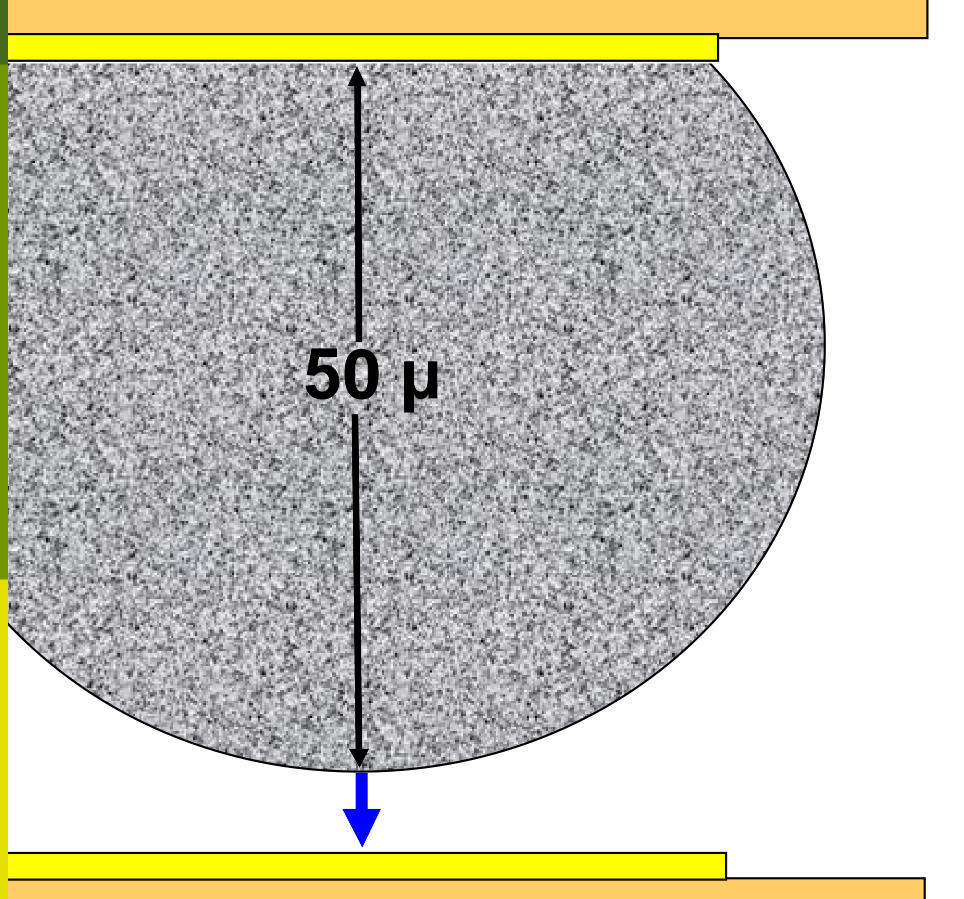
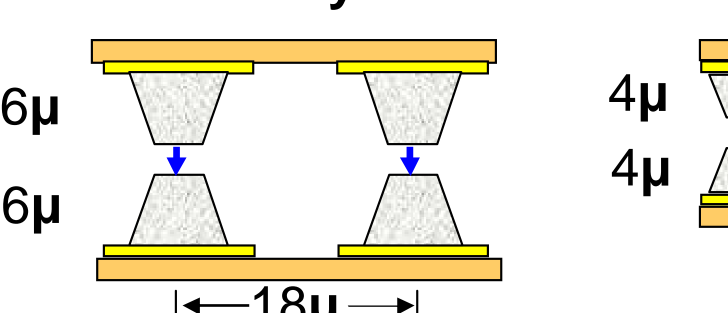
IR-FPA CHALLENGES: SMALLER PIXEL/BUMP SIZE → SIMILAR TO 3D-IC REQUIREMENTS

Conventional flip-chip solder ball

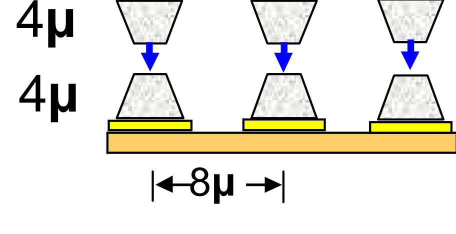


Indium-bumped IR-FPA

Today



Tomorrow

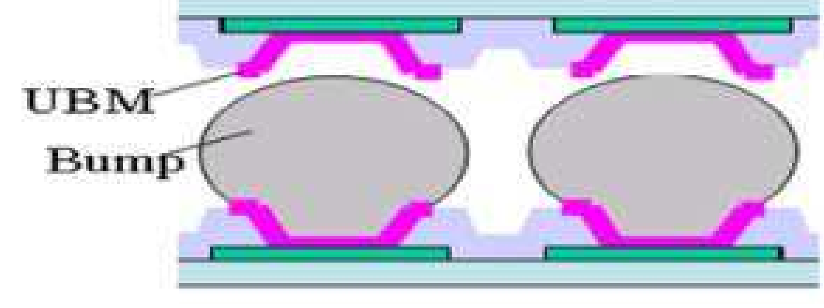


- **High Accuracy Parallelism and Alignment, Process Flexibility and Heterogeneous Integration are available**
- **High Throughput Required for 3D-IC adoption, still need to be addressed**

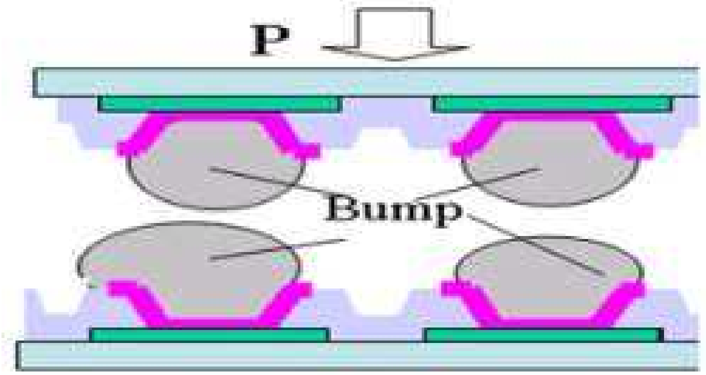
BONDING PROCESSES USED FOR IR-FPA ASSEMBLY

- There are 2 main families of FC joining techniques generally used to assemble heterogeneous imaging arrays

- Reflow Soldering



- Thermo Compression Bonding



BONDING PROCESSES USED FOR IR-FPA ASSEMBLY

- **Reflow Soldering**
  - T > Solder Melting Point
  - CTE Mismatch makes Alignment more and more difficult as Pitch decrease and chip size increase
  - Oxide protection or removal is required

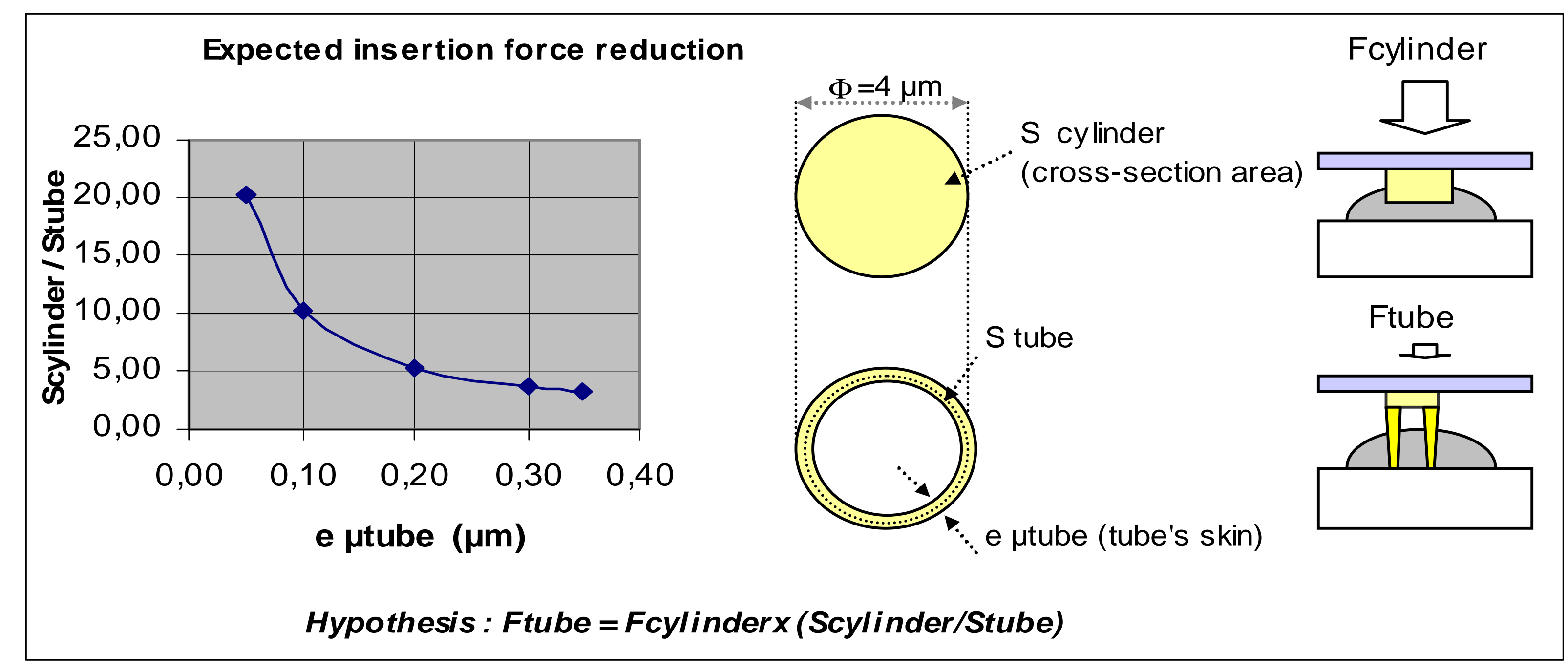
    (Presented at Imaps - Device Packaging 2008)
  - Die Warp and Smaller Bumps make Self Alignment reflow impossible

- **Thermo Compression Bonding**
  - T < Solder Melting Point
  - Force increases as the number of Pixel Number increases

    (over 3 tons on large state of the art IR-FPA for Aerospace)

THERMOCOMPESSION WITH INSERTION APPROACH

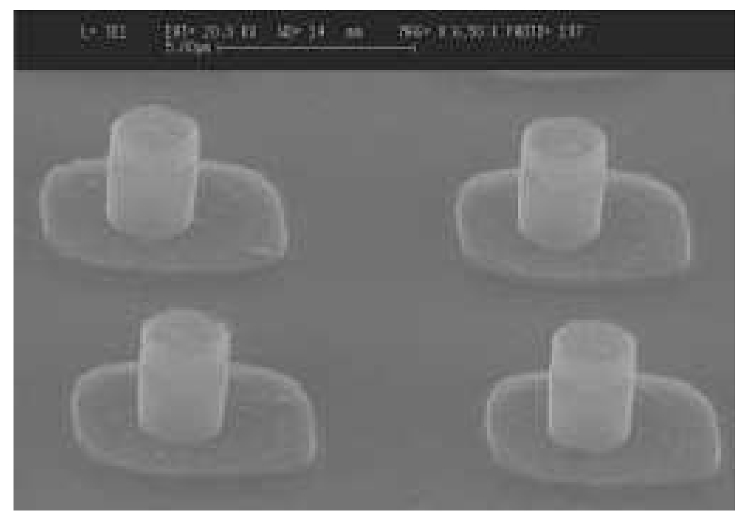
- Flip Chip Technique using micro-tubes and solder lands
- Ultrafine Pitch < 10 µm
- High Bumps Count (2000 x 2000) connections
- Adapted to heterogeneous imaging arrays fabrication

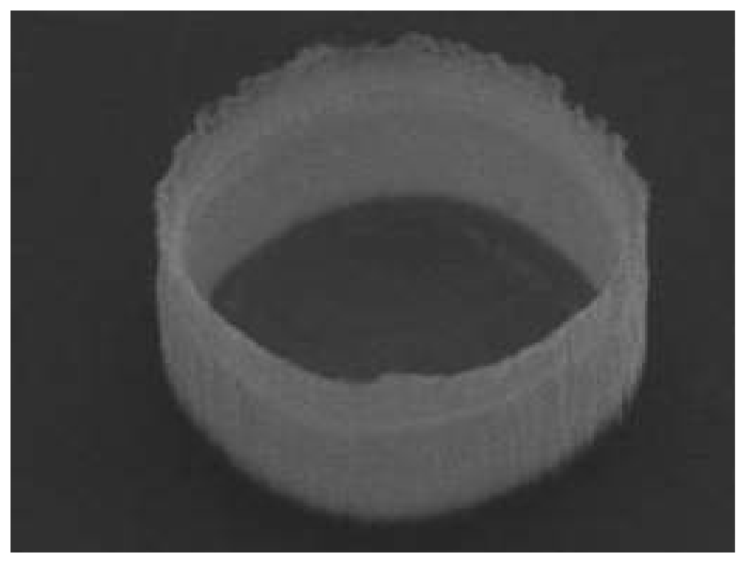


THERMOCOMPESSION WITH INSERTION APPROACH

- **Flux Less**
  - Gold plated µtubes break the native solder oxide establishing electrical contact
  - No flux cleaning is required
- **Low Pressure**
  - Sharp µtubes geometry and indium solder ductility, enable insertion at low force (<0.5mN/connection)
  - Can be handled by conventional FC Bonding equipment even for high very pin counts (i.e: >4 million connections)
- **Room Temperature**
  - No CTE mismatch issues
  - Bonding step can be completed by solid-solid diffusion

THERMOCOMPESSION WITH INSERTION APPROACH





- 4-million µtubes Array @ 10µm pitch
- Aligned on 6x6µm² metallic pads
- Different micro-tubes diameters with Height between **2.5 - 2.8 µm**

→ Die to Wafer Parallelism is critical to successful insertion and therefore bonding yield

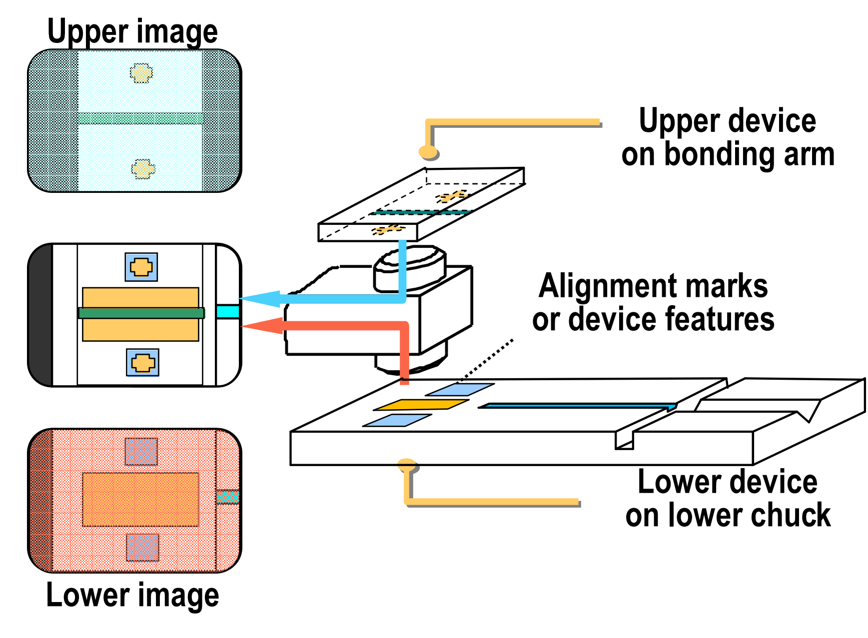
MACHINE USED FOR THE EXPERIMENT
SET FC300 - HIGH FORCE DEVICE BONDER

- ± 0,5 µm, 3σ Post-Bond Accuracy
  (Process dependent)
- Die Bonding, Flip Chip Bonding
- Large Device Bonding Capability
  - Device up to Sq. 100 mm
  - Substrate up to Ø 300 mm
- Process Flexibility
  - Up to 400 kg Bonding Force
  - Up to 450℃ Heating
  - UV-Curing, Ultra Sonic

FLIP CHIP ALIGNMENT & BONDING PRINCIPLE

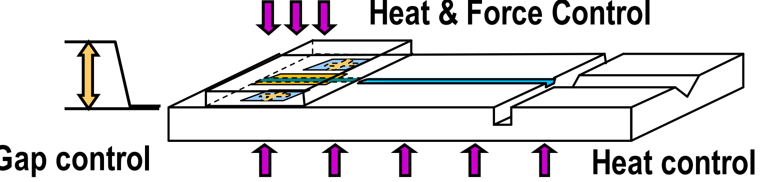
Step 1

- The Upper Die is loaded onto the bonding arm
- Wafer/Lower Die is loaded onto the chuck
- Through the upper blue optical path, the automatic alignment locates and centers the marks or features of the Die
- Through the lower red optical path, the automatic alignment aligns the marks or features of the wafer/Lower Die to the marks of the Upper Die



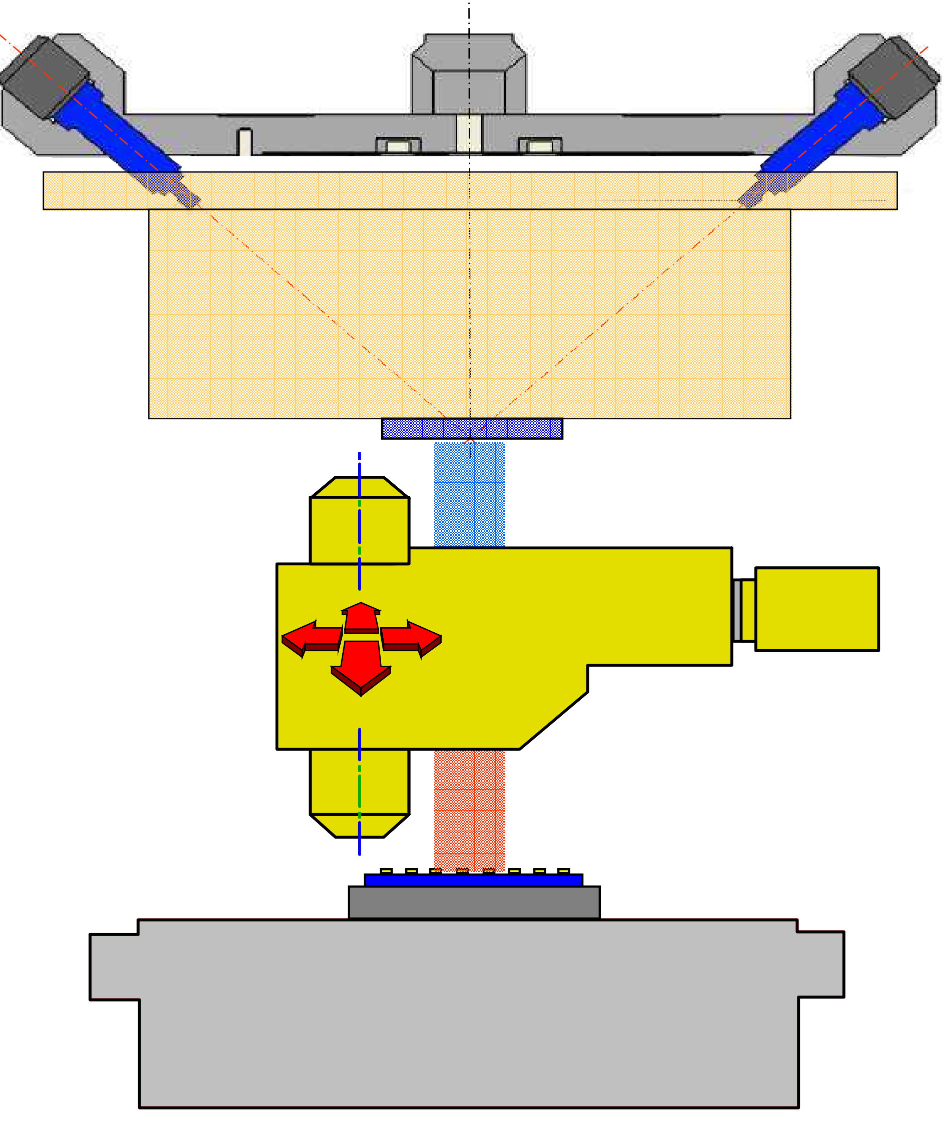
Step 2

- The bonding arm moves down to deposit/bond the Upper Die on the Wafer/Lower Die



ALIGNMENT AND BONDING SEQUENCE

- Die is secured by vacuum on a flat optically polished SiC Pick Up tool
- Parallelism is actively pre-adjusted using a motorized sphere coupled with an autocollimator (or laser leveling for IR-FPA)



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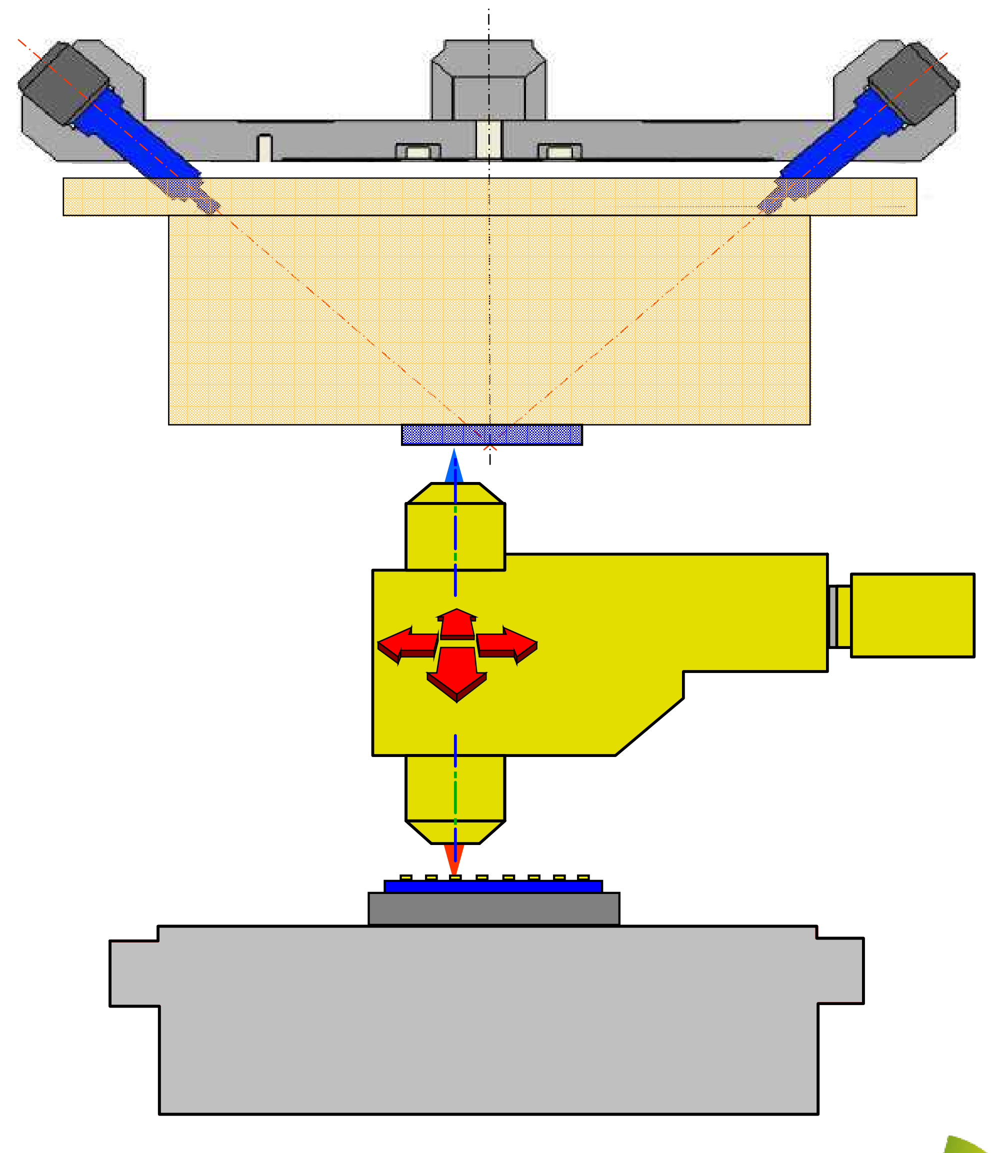

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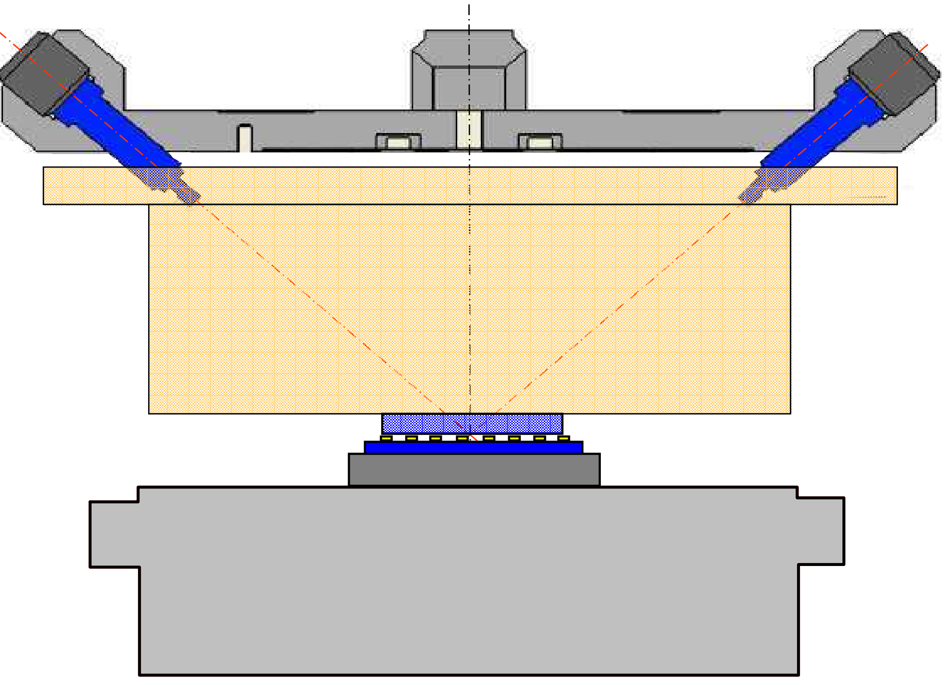
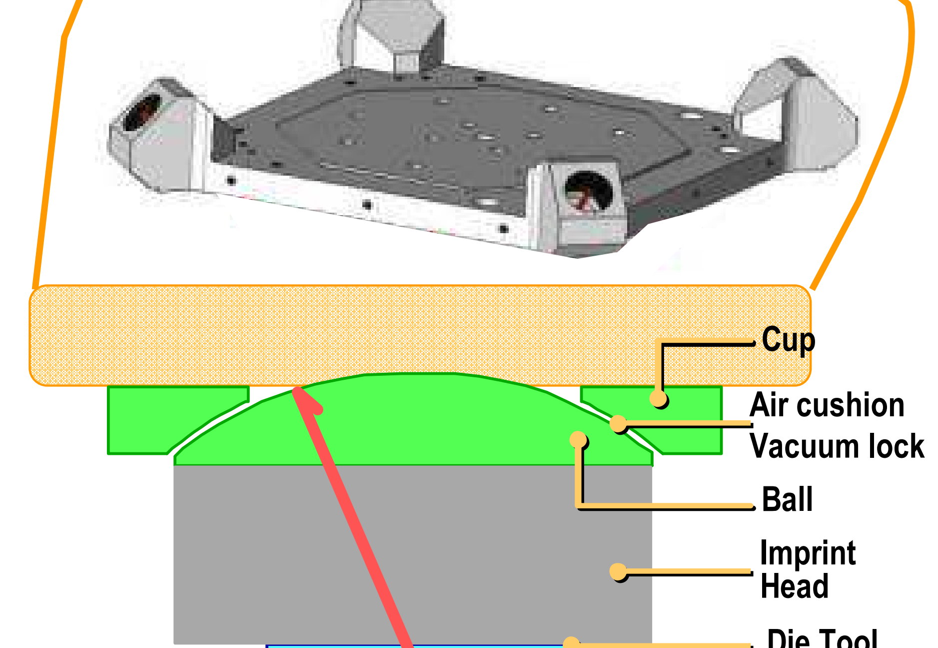


- Parallelism is finalized by Self Leveling during the bonding sequence when parts are into contact

PARALLELISM CONTROL



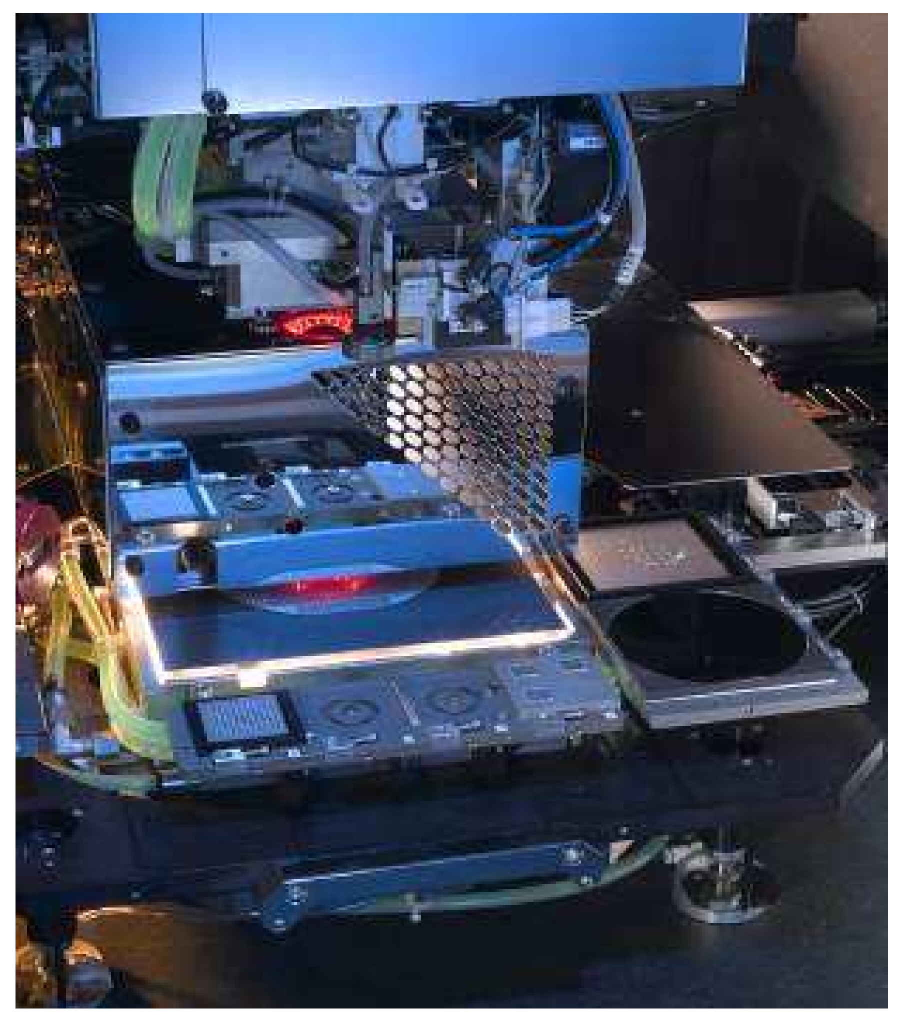
- **The Bonding Head includes a pre-leveling system**
  - Motorized Sphere
  - Active leveling resolution: 20 µradian
    → 1µm for 50mm Die
- **Final leveling is obtained by a flexure stage**
  - System sustains force up to 10,000N
  - Less than 500 grams force is required for self leveling (0.76mN.m/µradian)

→ ***Compatible with Low force as well as high force applications***

→ ***Self leveling may eliminate the need for pre-leveling which contribute to reducing the cycle time***

ALIGNMENT CONTROL

- **Alignment Optics**
  - Pixel equivalent: 0.67 µm
  - Autocollimator sensitivity: 20 µradian
  - → Attached to air bearing XY stage for parallelism stability
- **X, Y, Theta Axes**
  - Air bearing stage driven by linear motor, positioning controlled by optical encoder
  - XY resolution: 10nm
  - Theta resolution: 0.4µradian
- **Z Axis**
  - The most critical to get the accuracy together with the optical system
  - Resolution 50 nm
- **Interchangeable Bonding Head**



CONCLUSION

Various Developments conducted to meet the requirement of the IR-FPA evolution actually benefit to the 3D-IC Application

- **The Self Leveling System**
  - First introduced on the SET Nanoimprinting Stepper
  - Successfully adapted to bonding tool
  - → It will with no doubt contribute to good bonding when moving to direct bonding (Oxide/Oxide or Cu/Cu)
- **The Confinement Chamber for Oxide removal**
  - Presented last year at the Device Packaging Conference

- **High Speed Tool are available at lower accuracy**
  - → High Throughput at High Accuracy Bonding still need to be achieved