

## *Fabrication and performance of InAs/GaSb-based superlattice LWIR detectors*

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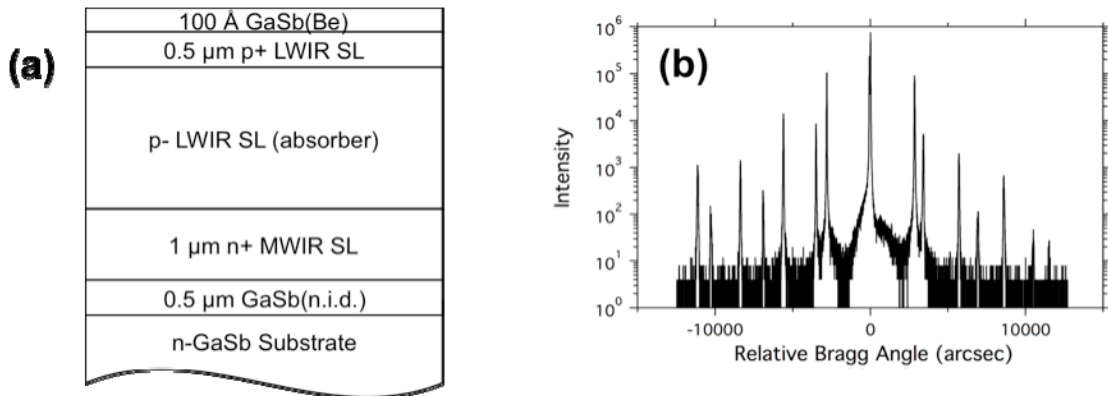
### INTRODUCTION

InAs/GaSb-based type II superlattices (T2SL) offer a manufacturable FPA technology with FPA size, scalability and cost advantages over HgCdTe. Work at Jet Propulsion Laboratory (JPL), Naval Research Laboratory (NRL), and Northwestern University (NWU) has shown that the performance gap between HgCdTe and T2SL FPAs has narrowed to within 5-10x over the last two years<sup>1,2,3</sup>. Due to the potential of T2SL technology for fabrication of large format (> 1k x1k) and dual-band arrays, HRL has recently resurrected efforts in this area<sup>4</sup>. We describe the progress on the FastFPA program funded by the Army Night Vision Labs towards the development of detectors and focal plane arrays (FPAs). Progress made in the areas of MBE growth, mesa diode fabrication, dry etch processing, and FPA fabrication over the last one year is presented.

### Material Characterization

Commercially available p-on-n ROICs were targeted for use for FPA fabrication. As such, a majority of the device results presented in this paper are for the p-on-n architecture. A majority of the devices used in this study were grown at HRL. Results from additional material provided by JPL and NRL for use on the FastFPA program are also discussed. The samples from HRL were grown in a VG V80 3" MBE system equipped with standard group III effusion cells and valved As and Sb cracker cells using 2" n-type GaSb(001) substrates. The detector was a basic p-on-n superlattice heterostructure design. Atop the 0.5  $\mu\text{m}$  GaSb buffer layer, the device consisted of a 1  $\mu\text{m}$  thick n+ MWIR SL region, followed by a lightly p-doped LWIR SL absorber layer, and then a 0.5  $\mu\text{m}$  thick p+ LWIR SL region. A thin 100  $\text{\AA}$  p+ GaSb cap was added for the top contact. The thickness of the absorber layer ranged from 1.3  $\mu\text{m}$  to 2.3  $\mu\text{m}$  in these samples. The MWIR and LWIR SL regions had nominal structures of 9 ML InAs/7 ML GaSb and 13 ML InAs/7 ML GaSb, respectively.

An illustration of the device structure and a typical XRD scan of that structure are shown in Fig. 1. There is a negligible mismatch between the SL-0 peak and the GaSb substrate, indicating the SL is nearly perfectly lattice-matched to the GaSb. The satellite peaks for both the LWIR and the MWIR SL layers are sharp with a FWHM of about 30 arc-sec or less for both types of layers.

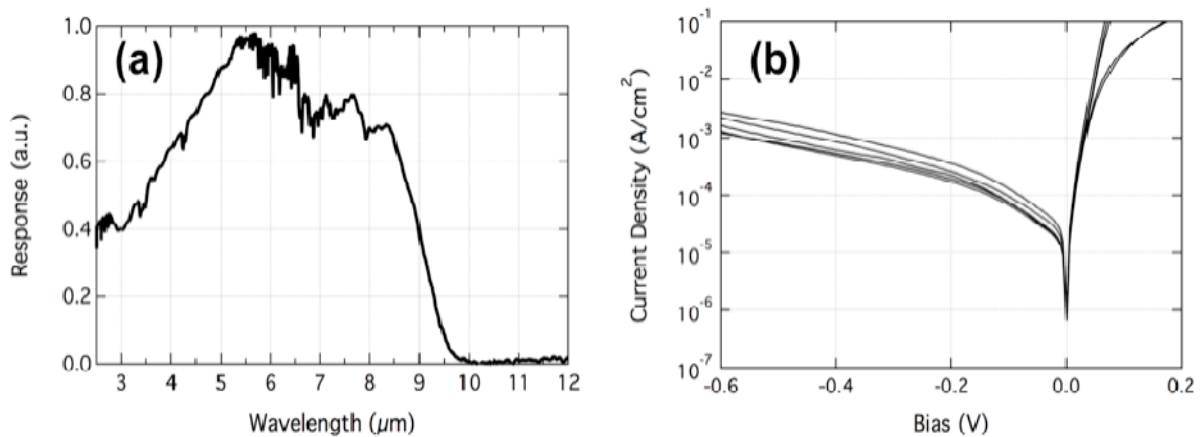


**Fig. 1:** (a) Illustration of the LWIR single-barrier heterostructure design. (b) XRD scan around the GaSb (004) reflection. The mismatch between the SL and GaSb is negligible, and the FWHM of the satellite peaks are 30 arc-sec or less.

Wet Etch Diode Fabrication

Variable-area discrete diodes were fabricated from SLS device structures using standard photolithography techniques and a citric acid based etch for mesa delineation. A single etch was used to both delineate the mesas and establish the common contact layer in the n+ SL layer. The test samples were mounted on leadless chip carriers (LCCs) from which a sampling of the various sized diodes were wire bonded using an Indium-ball bonding technique. After wire bonding, the samples were loaded into an LN<sub>2</sub> pour-fill dewar for testing.

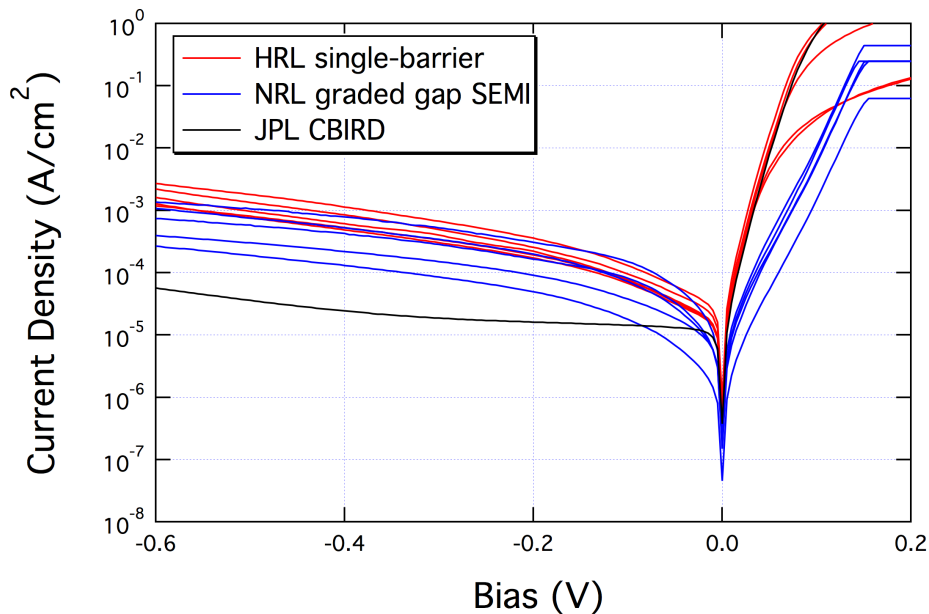
Representative characterization data from the large-area, unpassivated diodes are shown in Fig. 2. The spectral response was acquired using 200 μm x 200 μm diodes with top-side illumination. A typical spectral response for this structure, taken with a bias of -50 mV, is shown in Fig. 2(a) shows a cutoff wavelength of approximately 9 μm. The dark current measurements were acquired while using a cold shield to minimize the field of view of the devices. Typical results for various area diodes are shown in Fig. 2(b), where the square mesa dimension ranges from 75 μm to 200 μm.



**Fig. 2:** Typical characterization of the baseline LWIR structure from large-area diodes. (a) Spectral response showing a cutoff around 9 μm. (b) Dark current as a function of bias voltage for various diode sizes. The thickness of the absorber layer for this sample is ~2.3 μm.

Device wafers from the NRL and the JPL utilizing their advanced structure designs and MBE growth capabilities were also processed and characterized at HRL. The NRL material was an n-on-p design that utilizes the graded gap W-structure design and was processed using a shallow etch mesa isolation (SEMI) process as described by Aifer et al<sup>5</sup>. The JPL material was a CBIRD structure as described by Ting et al<sup>6</sup>, and was processed using a standard deep etch through the absorber layer.

The dark current densities as a function of bias measured from the HRL single-barrier p-on-n design are compared with discrete diode data from the processed NRL and JPL structures in Fig. 3. The HRL and NRL samples had a comparable cutoff wavelength of  $\sim 9 \mu\text{m}$ , while the JPL sample actually had a longer cutoff wavelength of  $\sim 10 \mu\text{m}$ . It is evident that the advanced device designs are critical in suppressing the dark currents in SLS detector structures. However, both the NRL and JPL designs require an electron-collecting ROIC for optimal device performance, and at present, there are no such commercially-available ROICs suitable for SLS detectors based on their current performance levels. Thus, in order to continue the development of an FPA fabrication capability at HRL, the HRL-grown single-barrier (p-on-n) structures were used with the ISC9705 ROIC from Indigo.



**Fig. 3:** A comparison of dark current density measurements taken from large-area discrete diodes from HRL, NRL, and JPL samples. The advanced NRL and JPL designs show a reduction in the dark current, but their architectures require electron-collecting ROICs.

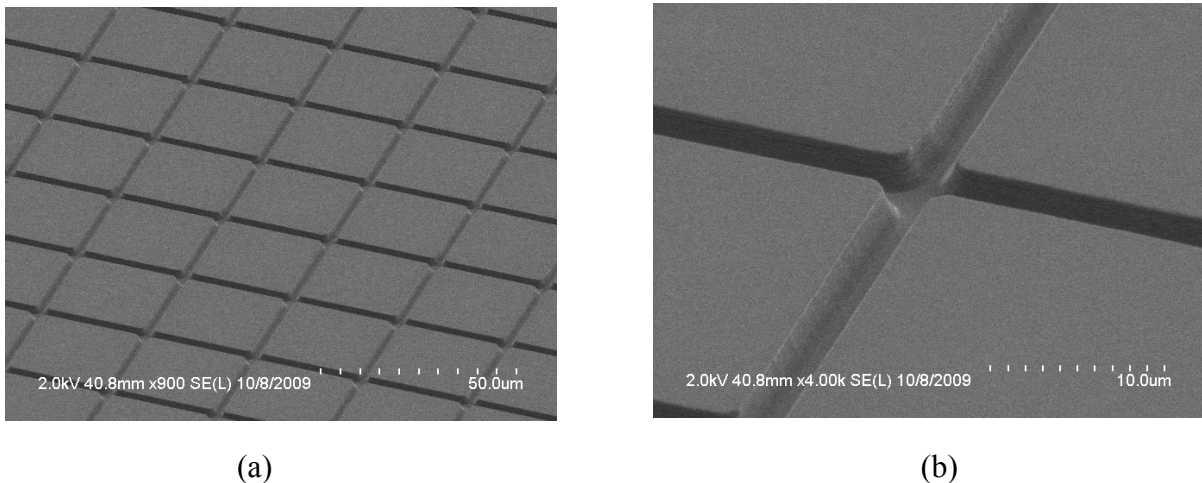
### Dry Etch

A dry-etch based process is needed to achieve either high-aspect ratios ( $>5:1$ ) or uniform etch depths across a large portion of the wafer. The ability to fabricate structures

with high aspect ratios is especially important for high fill factor (>85%), and small pitch (~18 $\mu\text{m}$ ) for dual-band detectors which require a deep etch for pixel isolation. Lateral uniformity of etch depth uniformity is important for the fabrication of large arrays (>1Kx1K) that require a shallow etch mesa isolation (SEMI). To minimize exposure of the narrow band gap region within the sidewall, etch depths for SEMI process has to be controlled. The merits of T2SL technology are likely to challenge HgCdTe from cost and performance standpoints especially for advanced detectors (3<sup>rd</sup> generation dual-band or large format arrays). The development of a satisfactory dry etch process is therefore important for continued progress of T2SL technology.

Experiments were carried out to investigate and develop a dry etch process for the fabrication of mesa device structures on FPA-type patterns. Various gas mixtures were developed to etch the superlattice epilayer, and create mesa diodes. Figure 4 shows a 30 $\mu\text{m}$  pitch array with 27 $\mu\text{m}$  size pixels. The fill factor for this configuration is 81% with an aspect ratio of the etched trench at roughly 3.4-to-1 with smooth morphology at the side-walls as well as at the bottom of the mesa region.

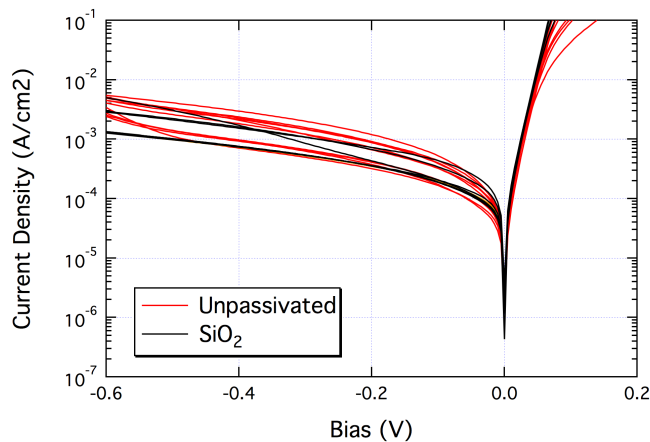
The detectors processed from these dry-etched wafers show performance characteristics nearly an order of magnitude less than wet-etched mesa detectors in terms of dark current. This suggests that there exists some deleterious effect due to the dry-etch process which incorporates some damage, and thus, further optimization is required to improve devices performance. Various clean-up etches are presently being explored to remove the damaged sidewall material and reduce the dark current, and restore the diode performance.



**Figure 4. (a) SEM images of dry-etched T2SL epilayer with high fill-factor FPA layout comprised of 27 $\mu\text{m}$  detectors and 3 $\mu\text{m}$  streets. (b) Close-up image shows an aspect ratio over 3-to-1 with smooth morphology at the side-walls and on the bottom surface.**

## FPA FABRICATION

The fabrication of the 320x256 format FPA's was carried out on HRL-grown material. Mesa patterns were generated using standard contact photolithography with 27 $\mu\text{m}$  wide detectors on a 30 $\mu\text{m}$  pitch layout. A standard citric etch solution was used to delineate the mesa devices. Once the mesa patterns were etched, PECVD SiO<sub>2</sub> passivation was deposited using a mixture of silane and nitrous oxide. The SiO<sub>2</sub> passivation typically yields performance characteristics similar to that of unpassivated diodes as shown in Figure 5. Image-reversed photolithography was used to deposit Ti and Au for both the top and bottom contact.



**Figure 5. Comparison of passivated and unpassivated diodes.**

One of the challenging steps in the processing of the FPAs is the thick photoresist lithography necessary for the indium bump evaporation. Several iterations were necessary to optimize the photoresist conditions in order to yield a uniform thick lithography pattern. The advantage of using this approach, however, is that the photolithography can be carried out in one step, as opposed to preparing multi-layers of photoresists to achieve a thick pattern.

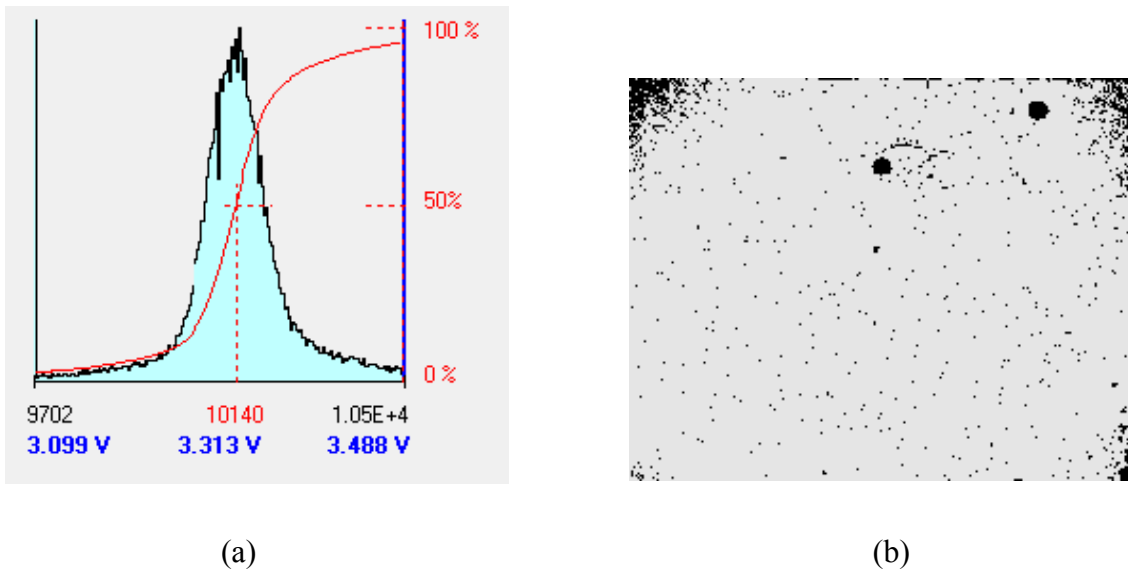
Indium bumps were subsequently deposited using a thermal evaporator configured with a large crucible with enough indium pellets necessary to deposit 8 $\mu\text{m}$  tall bumps. Once the lift-off was carried out, the wafer was re-coated with a blanket of thick photoresist to protect the indium bumps during dicing of the individual FPAs. A Suss/SET FC300 was used to hybridize the focal plane arrays onto a FLIR(Indigo) 9705 series ROIC's. The accuracy of this instrument is on the order of 0.5 $\mu\text{m}$ , and a series of collimation steps were necessary to achieve an accurate alignment.

The hybridized parts were mounted on an 84-pin LCC, wire bonded, and then loaded into a LN<sub>2</sub> pour-filled dewar rated at 80K. An SEIR test station was used to drive the 9705 ROIC and characterize the FPA. For these initial assessments, the GaSb substrate was not removed, and no epoxy backfill in between the indium bumps was carried out. As a result,

only preliminary FPA characteristics were extracted prior to the gradual de-lamination of the FPA from the silicon ROIC due to thermal cycling of the FPA assembly.

### FPA Characterization

FPA testing was performed without a cold shield or any narrow pass filter. A histogram of the DC response of the FPA to a set bias is shown in Fig. 2(a), with a  $\sigma$ /mean of about 4.7% for all the pixels in the 320x256 array. A two-dimensional map of the pixel outages is shown in Fig. 6(b), with an operability of 95.9%. Much of the outages are from the corners that are due to the de-lamination, as this data was taken after four cool down cycles.



**Figure 6. (a) DC output histogram for all the pixels, and (b) two-dimensional defect map for the hybridized array.**



**Figure 7. Broad-band LWIR image taken from the superlattice 320x256 Focal Plane Array using pixel substitution.**

### *SUMMARY*

Rapid progress has been achieved at HRL on the InAs/GaSb-based type-two superlattices over the period of nine months. A baseline citric acid based wet etch process was developed for processing shallow and deep etched discrete and FPA format pixels. In addition, a reliable PECVD-based SiO<sub>2</sub> passivation processes was established. These processes were used to fabricate a prototype 320x256 format FPA assembly using a commercially available ISC9705 ROIC. An HRL-grown simple heterojunction p-on-on wafer was used for the initial FPA demonstration. IR imagery as well as preliminary FPA operability was generated in the effort. A dry etch process which can be used for both single color as well as future dual-band fabrication was developed. Our halogen-based dry-etch process provided etch rate of 2.3 $\mu$ m/hr and was verified for a near 100% optical fill factor 30 $\mu$ m pitch FPA layout.

### *Acknowledgements*

We thank Meimei Tidrow and the US Army NVESD for supporting the effort. We also thank Lucy Zheng (IDA), Leslie Aitcheson (NVESD), Cory Hill (JPL) and Ed Aifer, Jerry Meyer and Chad Canedy (NRL) for their help and support.

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